

Editorial

Jan van Schoot* and Helmut Schift

Next-generation lithography – an outlook on EUV projection and nanoimprint

DOI 10.1515/aot-2017-0040

Lithography is dead – long live lithography! For years, optical lithography has been the workhorse for high-volume manufacturing (HVM) of sophisticated semiconductor chips used for data processing and storage. The need for smaller and smaller structures has called for new patterning solutions, some of them involving the extension of existing optical principles, parallel patterning, and step and repeat by covering the surface of silicon wafers with consecutive exposure of identical patterns, projection of demagnified patterns from a mask onto the wafer instead of proximity printing. Others are employing different physical concepts from using massive parallel electron beams or even mechanical imprinting of resists, which sound like falling back into the times almost 600 years ago when Johannes Gutenberg invented book printing with movable metal letters.

In a time of calls for disruptive changes, the most important news is that nothing is stable, except change. At the same time, technologies continue to determine entire landscapes of production for years, and one of those is optical lithography. What has been will be again, what has been done will be done again; is there nothing new under the sun? The ability of engineers to cope with requirements of ongoing miniaturization, all because of the economic laws of growth, is amazing. But now, 2017, optical lithography – as we know it – might be near replacement. Funny enough, it is not the physical law calling for it. Multiple patterning with over four masks for single layers in semiconductor device processing is simply so complex and expensive that it will continue to be employed for the next ‘node’ (N7, i.e. 7-nm resolution), the design resolution that defines the progress toward higher resolution.

But different from expected, the current solutions are still using most of the ingredients of traditional optical lithography. In 1986, Hiroo Kinoshita proposed the use of extreme UV (EUV) as the consequent continuation of photolithography with smaller wavelengths, which means 13.5 nm instead of 193 nm from deep ultraviolet (DUV) [1]. However, instead of transmission lenses, mirrors have to be used; also, the mask has to be operated in reflective mode. EUV projection lithography (EUVL) will enable to go back to single mask exposure instead of double or quadruple exposure, at least for the coming node N7 and later N5 (see also Figure 1) [2].

The leading semiconductor manufacturers are making now the transition toward putting EUV lithography into production [3]. The current exposure tools exploit a numerical aperture (NA) of 0.33 [3]. Beyond N5, it is foreseen that with this NA, double patterning is needed again. At this very moment, a high-NA anamorphic EUV projection system is being developed [4, 5] and will push the NA toward 0.55, enabling N3 and beyond to be printed with the same EUV wavelength using a single mask exposure.

For EUVL, so far, the highest hurdle was the needed power of the 13.5-nm light source to enable economical production capacity of the exposure tools. Recent publications [6] show that the needed power of about 200 W is now demonstrated, needed for 125 wafers of 300-mm size per h. In this issue, an overview of the progress in the EUV light source is given by Igor Fomenkov from Cymer/ASML. There are, however, other areas where a lot of work is being done to bring EUV to the very demanding requirements of a HVM environment.

First of all, there is the so-called mask-3D effect. Structures at the mask are becoming so small relative to their thickness that this shadowing-like effect is not negligible anymore. How to overcome this effect will be described by Andreas Erdmann from the Fraunhofer Institute IISB in his contribution.

Especially in patterning masks for the future high-NA tools, mask writing becomes more complicated because of the decrease in critical feature size and the anamorphic projection optics, changing the aspect ratio on the mask. Methods to deal with this are described by Stephen Hsu

*Corresponding author: Jan van Schoot, ASML Netherlands BV, System Engineering and Research, De Run 6501, Veldhoven 5504 DR, The Netherlands, e-mail: jan.van.schoot@asml.com

Helmut Schift: Paul Scherrer Institut, Laboratory for Micro- and Nanotechnology (LMN), Villigen PSI 5232, Switzerland

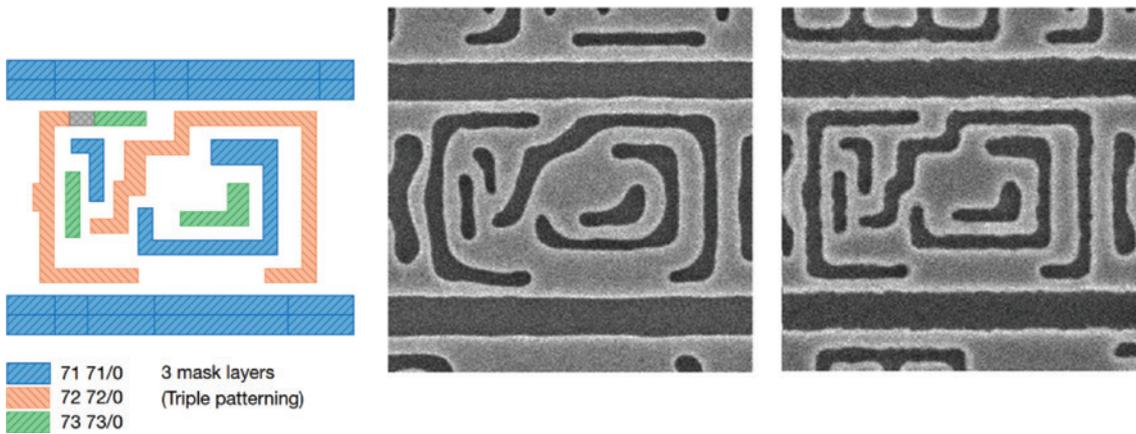


Figure 1: The mask template and two SEM images of 24-nm structures of a 10-nm-node standard logic cell, exposed in different ways. The SEM image on the left was exposed using 193-nm immersion, triple exposure. On the right, a EUV single-exposed image is shown. Note also the better defined image with the EUV exposure [2] (Figure courtesy Greg McIntyre, IMEC).

from Brion/ASML. A third critical area at the mask is to make and keep it defect free. An overview of the different types of mask defects and the current state of art is described by Rik Jonckheere from the IMEC institute in Leuven.

During the use of the mask, new defects can occur by particles falling onto the mask. Derk Brouns from ASML describes the so-called pellicle: a thin membrane that covers the entire mask area in order to keep these particles out of the focal plane and avoid printing.

Now our photons, generated in the source, and at the well-protected mask given its information, travel through the projection optics towards the wafer where they are supposed to transfer the image into a photosensitive layer or resist. Again, there is a broad area of investigations, especially toward the future where the structures to be printed are so small that the statistics of the small number of photon printing are becoming important. In the article of Danilo de Simone from IMEC, an overview of this field will be given.

Nanoimprint lithography (NIL) was invented and demonstrated in the 1970s by Susumu Fujimori at NTT in Japan, but it was not until 1995 when Stephen Chou and co-workers at the University of Minnesota (later at Princeton University) published their first results that NIL started to gain broader attention, by demonstrating 10-nm-imprint capabilities at a time when 50 nm was considered as the resolution limit of projection lithography (see Figure 2) [7, 8]. At that time, X-ray proximity lithography (using 1.3-nm wavelength) was seen as an alternative to DUV projection, using 248-nm light from KrF-excimer lasers.

From the beginning, NIL was considered as an alternative for DUV-based projection lithography for IC-chip fabrication. The UV-assisted NIL process – in contrast to

Chou's thermal NIL – was established at the same time by Jan Haisma from Philips in Eindhoven and nearer to traditional optical lithography because it employed photocurable resists instead of the more general thermoplastic materials [9]. Further developments followed. One of the most important is the step and flash imprint lithography (S-FIL) invented by the University of Texas in Austin and commercialized by Molecular Imprints Inc. (MII) [10].

In 2003, NIL was named as one of the 'ten emerging technologies that will change the world' by the MIT Technology Review, and the technique was added to the ITRS roadmap for the 32- and 22-nm nodes. When it was time for the industry to switch to the 22-nm node, it chose to stick with DUV projection lithography. But NIL remained on the ITRS roadmap for smaller nodes, and many believed that NIL can replace DUV-lithography in manufacturing as the main competitor to EUVL. 'Next-generation lithography' NIL is, however, not only used in areas where HVM by lithography is already established, but also where patterning becomes affordable, including research areas where expensive processes could not be used. Important contributions to a wide field of applications were done via collective approaches, e.g. in European large-scale projects such as NaPa and NaPANIL and via national programs in Korea, Japan, Taiwan, and Singapore [11, 12].

Different companies have contributed to the development of NIL for HVM. Furthermore, various tool concepts have been developed to fulfill the needs of customers (research, industry) and end users (focused or wide range of applications). Although often different in terms of capabilities and processes, the basic concepts have much in common, and many efforts have been undertaken to adapt different processes to the requirements of various

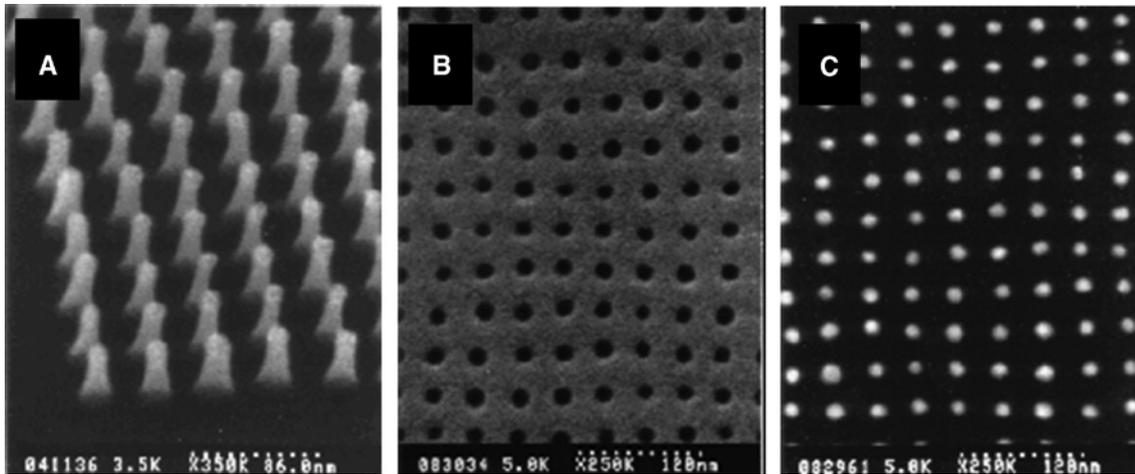


Figure 2: The initial demonstration of thermal NIL by Stephen Chou and co-workers in 1997 showing the NIL process chain. SEM micrographs: (A) SiO_2 stamp with pillars of 10-nm diameter, 60-nm height, and 40-nm period; (B) imprinted pattern into a thermoplastic film (PMMA resist); (C) 10-nm metal dots after lift-off process (Reprinted with permission from Ref. [8]. Copyright (1997) American Vacuum Society).

applications. The only one heading toward HVM of semiconductor devices was S-FIL, now rebranded J-FIL (jet and flash imprint lithography). At the same time, MII put much effort into the development of other key applications such as patterned sapphire substrates or patterned magnetic media.

Then, in 2014, Canon Nanotechnologies Inc. (CNT) acquired MII with its core J-FIL technology. Particularly after this decisive step, NIL was again considered as a main contender for HVM of semiconductor devices. Strategic partnerships with Toshiba and Hynix aim to test NIL under production conditions. Toshiba, e.g. is currently testing both EUVL and NIL for production of NAND flash memory. The next years will show whether NIL will be able to compete with EUVL or complement it in areas where cost issues become dominant.

Therefore, this special edition collects a range of NIL tools, and – as an example of a process with a quite different approach – interference lithography: Douglas Resnick and Jin Choi from Austin-based CNT present a conclusive review of NIL for high-volume semiconductor device manufacturing. This is particularly important because the paper presents the cumulative achievements made within more than 10 years of development at MII and after integration into the framework of next-generation semiconductor lithography systems at CNT.

CEA-Leti and EV Group GmbH has teamed up and launched the INSPIRE program (Imprint Nanopatterning Solution Platform for Industrial Assessment), which aims at building a nanoimprint solution platform for industrial assessment and provide a unique open ecosystem for the standardization of the nanoimprint process. It is the first

paper in which Hubert Teyssedre and his colleagues are presenting an assessment of the capabilities of the newly delivered EVG HERCULES 200-mm industrial platform at the premises of CEA-Leti in Grenoble.

The concept of soft, bendable stamps has been employed by the substrate conformal imprint lithography (SCIL), developed by Philips Research. The new platform currently established by Philips SCIL Nanoimprint Solutions, is intended for large-area imprint. The paper from Marc Verschuuren and his colleagues is a review on the technology and achievements of SCIL for various applications.

The paper about laser interference patterning (LIP) methods by Andrés Lasagni from the Technical University of Dresden is a classical review on the possibilities for high-throughput fabrication of periodic surface patterns. Different from resist-based interference lithography, he also presents ablation by high-intensity laser beams. This opens way for the fabrication of micro- and nanostructured cylinders for roller imprint.

EUVL is a clear example demonstrating that the road from lab to fab can be bumpy and longer than anticipated. However, after the significant progress with masks, resists, and EUV light sources over the last years, EUVL is now being adapted as the next HVM lithographic technology for future IC chip manufacturing. At the same time, other techniques are further developed. In comparison to many other techniques that have vanished after industry has chosen their favorite tool, NIL, together with other processes such as interference lithography, is still under investigation. The progress of NIL in terms of defectivity already enabled its use in less-critical segments such as

high brightness LEDs and VCSELs, and potentially in photovoltaic cells and biosensors. Some chip manufacturers are starting to test NIL for non-volatile memory.

The promising progress in EUVL with high-NA on the roadmap, and in emerging alternatives like NIL will help to continue Moore's law in the coming decade. May lithography live forever!

References

- [1] H. Kinoshita, K. Kurihara, Y. Ishii and Y. Toriie, *J. Vac. Sci. Technol. B* 7, 1648 (1989).
- [2] B. Vandewalle, B. Chava, S. Sakhare, J. Ryckaert and M. Dusa, *Proc. SPIE* 9053, 90530Q (2014).
- [3] B. Turkot, S. Carson, A. Lio, T. Liang, M. Phillips, et al., *Proc. SPIE* 9776, 977602 (2016).
- [4] J. van Schoot, K. van Ingen Schenau, G. Bottiglieri, K. Troost, J. Zimmerman, et al., *Proc. SPIE* 9776, 977611 (2016).
- [5] J. van Schoot, K. Troost, S. Migura and B. Kneer, *SPIE Newsroom*, 12 January (2016). Available at: <http://spie.org/x116763.xml>.
- [6] A. Schafgans, D. Brown, I. Fomenkov, Y. Tao, M. Purvis, et al., *Proc. SPIE*. 10143 (2017).
- [7] S. Fujimori, *Jap. J. Appl. Phys.* 48, 06FH01 (7 pp) (2009).
- [8] S. Y. Chou, P. R. Krauss, W. Zhang, L. Guo and L. Zhuang, *J. Vac. Sci. Technol. B* 15, 2897–2903 (1997).
- [9] J. Haisma, M. Verheijen, K. van den Heuvel and J. van den Berg, *J. Vac. Sci. Technol. B* 14, 4124–4128 (1996).
- [10] M. Colburn, S. Johnson, M. Stewart, S. Damle, T. Bailey, et al., *Proc. SPIE* 3676, 379–385 (1999).
- [11] H. Schiff and A. Kristensen, in: 'Handbook of Nanotechnology', third edition, Ed. By B. Bhushan (Springer Verlag Berlin Heidelberg, Germany, 2010). ISBN: 978-3-642-02524-2, XLVIII, with DVD, 271–312.
- [12] H. Schiff, *J. Vac. Sci. Technol. B* 26, 458–480 (2008).



Jan van Schoot

ASML Netherlands BV, System Engineering and Research, De Run 6501, Veldhoven 5504 DR, The Netherlands
jan.van.schoot@asml.com

Jan B.P. van Schoot, PhD, is senior principle architect at ASML, department of System Engineering. He is based in Veldhoven, The Netherlands. Van Schoot studied Electrical Engineering at the Twente University of Technology. He received his PhD in Physics on the subject of non-linear optical waveguide devices in 1994. After his graduation he held a post-doc position in cooperation with British Telecom and Flamel Technologies, studying a waveguide based electro-optical modulator. He joined ASML in 1996. In 1997 he became Project Leader for the Application of the first 5500/500 scanner as well as its successors up to the 5500/750. In 2001 he became Product Development Manager of Imaging Products (DoseMapper, Customized Illumination). Since 2007 he joined the department of System Engineering. He was responsible for the Optical Columns of the NXE:3100 and NXE:3300 EUV systems. After this he worked on the design of the EUV source. Currently he is the study leader of the High-NA EUV system. He holds over 20 patents in the field of optical lithography and presents frequently at conferences about photo lithography.



Helmut Schiff

Paul Scherrer Institut, Laboratory for Micro- and Nanotechnology (LMN), Villigen PSI 5232, Switzerland

Helmut Schiff is head of the Polymer Nanotechnology Group in the Laboratory for Micro- and Nanotechnology (LMN) at the Paul Scherrer Institut (PSI) in Villigen, Switzerland. He studied electrical engineering at University of Karlsruhe, Germany, and the École Nationale Supérieure de Physique de Strasbourg (ENSPS), France, and performed his PhD studies at the Institute of Microtechnology Mainz (IMM), Germany. After his graduation in 1994, he joined PSI as a research staff member. His work includes all aspects of replication technology, from 3D stamp manufacturing to polymer nanorheology. Since more than 20 years he is involved in the development of nanoimprint lithography (NIL) as an alternative nanopatterning method and has worked in national and international projects. In 2015, during the celebration of 20 years of Nanoimprint Lithography, he was awarded the Nanoimprint Pioneer Award.