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Microchip Transfer Process for Implantable Flexible Bioelectronic Devices

Abstract: The demands on flexible implants for recording of neural signals and electrical stimulating have increased in recent years with regard to their functionality, miniaturization, and spatial resolution. These requirements can be met best by embedding powerful complementary metal oxide semiconductor (CMOS) microchips into thin biocompatible polymer substrates. So-called chip-in-foil systems thus combine mechanical properties of a polymer substrate and performance of CMOS technology.

The development of a process for direct transfer of multiple CMOS microchips (edge length $<400\text{ }\mu\text{m}$) simultaneously into thin polyimide (PI) substrates is subject of this study. It allows the use of standard microelectromechanical systems (MEMS) processes for further levelled superficial layer build-up. This is achieved with the help of a silicon carrier wafer equipped with cavities for precise chip placement and a sacrificial layer to facilitate release of the chip-in-foil systems. In a post-processing step all silicon chips are thinned down to $100\text{ }\mu\text{m}$.

With this process a transfer yield of 100 % ($n = 34$) was achieved for the silicon chips on a die level. Chip rotational error on substrates was determined to be as low as $0.21^\circ \pm 0.10^\circ$. Die adhesion was examined by shear tests, resulting in shear strength of $58.1\text{ MPa} \pm 13.7\text{ MPa}$, which dropped to $15.2\text{ MPa} \pm 10.5\text{ MPa}$ after accelerated ageing in 60°C phosphate buffered saline solution (PBS) for 16 days (equivalent to 78 days at 37°C).

This study demonstrated a reliable microchip transfer process with low positioning error into flexible PI substrates with post-processing thinning of the dies. The use of a carrier silicon wafer allowed precise electrical interconnect

fabrication with standard MEMS processing techniques and without handling of thin and fragile chips. These results are a prerequisite to meet needs of reliability and structural biocompatibility in implantable flexible bioelectronic devices.

Keywords: Polyimide, neural implants, chip-in-foil system, thin-film, microchip, transfer

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1 Introduction

Neural electrodes are frequently used for recording and stimulation in the central and peripheral nervous system to help physically impaired patients in their everyday life [1, 2]. Improving functions of such implantable devices often results in complexity increase, as for higher spatial resolution and selectivity e.g. high-density electrode arrays are required [3].

Keeping a small form factor to minimize invasiveness of such implants while also maintaining conformability and biocompatibility to guarantee adequate host response is challenging. Complex integrated circuit systems (ICs) can be realized in thin complementary metal oxide semiconductor (CMOS) microchips and transferred into flexible thin-film polymer substrates with integrated metal interconnects [4, 5]. The combination of both allows for CMOS performance with conformability of polymer-based substrates [4]. Chip-in-foil systems thus pose a viable solution, but additional challenges in embedding multiple microchips and their alignment arise.

This work presents a reliable approach of a fabrication process for chip-in-foil systems with accurate chip positioning and the optical and mechanical characterization by shear testing of the final samples.

2 Materials and Methods

Therefore, a novel scalable approach to transfer multiple microchips simultaneously into thin polyimide-based flexible substrates has been developed (Figure 1). Microchips are first to be positioned individually and aligned with high accuracy

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by means of a carrier wafer provided with dry etched cavities. Fixing the chips in their position and rotation, as well as adjusting the chip height to the carrier wafer by grinding, allows superficial layer build-up with standard microfabrication techniques (e.g. photolithography, physical vapor deposition) in an all-in-polyimide process.

2.1 Transfer process

The transfer process started with the fabrication of the carrier silicon wafer. Cavities were dry-etched into a 4" silicon wafer by deep reactive ion etching (DRIE) (STPS Technologies, United Kingdom), into which the microchips were later inserted. Dimensions and shape of the cavities determine the position and orientation of the chips in the final devices. The wafer was then coated with a 15 μm thick sacrificial layer of copper (Cu) by electroplating. UV-light-deactivated tape (E5125 KL, LINTEC Corporation Advanced Materials Operations, Japan) was applied to which the chips' front sides adhere for further initial processing (Figure 1(i)). After manual placement, the chips were levelled to the backside of the carrier by grinding (DAG 810, Disco Corporation, Japan). Next, 5 μm of polyimide (PI) (BPDA-PPD) were applied to the back side by spin-coating and soft-cured at 90 $^{\circ}\text{C}$ for 5 min. The chips were held in place by the PI, allowing the removal of the front side UV-tape after UV-light exposure (Figure 1(ii)). The PI was then fully cured at 450 $^{\circ}\text{C}$ for 10 min, after which the final devices' layers were added on top as follows: First, 5 μm of PI were spin-coated and soft-cured at 90 $^{\circ}\text{C}$ for 5 min, then fully cured at 450 $^{\circ}\text{C}$ for 10 min. Covered microchip contact pads were opened by reactive ion

etching (RIE) with oxygen plasma (STPS Technologies, United Kingdom). AZ5214 E image reversal resist (MicroChemicals GmbH, Germany) was spin-coated, exposed, and developed on top, followed by an O_2 flash in an RIE machine (80 W, 30 s). A gold (Au) and tungsten-titanium (WTi) stack (50 nm WTi, 300 nm Au, 50 nm WTi) was sputter deposited in an Ardenne CS730 (Von Ardenne GmbH, Germany). Excess material was removed by lift-off in dimethyl sulfoxide (DMSO), isopropanol, and deionized (DI) water. After performing an O_2 flash (80 W, 30 s), a 5 μm insulating top layer of PI was spin-coated and fully cured as already explained earlier in the paragraph (Figure 1(iii)). Back side PI was then removed, followed by opening fan-out contact pads and separation of the individual samples, all done by RIE. Prior to back side grinding down the microchips and carrier wafer to the desired thickness of 100 μm , E3215 KL tape was added to the front side for added stability and protection (Figure 1(iv)). Finally, after UV-light exposure the tape was removed and the devices released by selectively etching the Cu layer in Cu(II)-Cl solution at 45 $^{\circ}\text{C}$ and rinsing with DI water (Figure 1(v)).

2.2 Process evaluation

For process evaluation square-shaped microchips (390 x 390 μm^2) equipped with basic test structures were transferred in this study. Correct orientation during manual placement was ensured by rounded corners of the dies, one corner having a noticeably larger radius of curvature. Test structures consisted of 300 nm sputtered aluminum metal interconnects with contact pads as small as 60 x 60 μm^2 and 90 x 90 μm^2 .

Transfer yield was analyzed by counting the amount of successfully transferred microchips after device release. Rotational positioning error was analyzed optically using the GIMP software (gimp.org, The GIMP Development Team, USA). Shear tests were conducted in a DAGE4000 Multipurpose Bondtester (Nordson DAGE, United Kingdom) with a 10 kg cartridge (test speed: 200 $\mu\text{m}/\text{s}$, shear height: 50 μm) to acquire information about adhesion performance of transferred dies to the PI substrate. Individual samples were subjected to thermal aging in phosphate buffered saline (PBS) solution for 16 days at 60 $^{\circ}\text{C}$ (corresponding to 78 days at 37 $^{\circ}\text{C}$ [6]) in an incubator (Heraeus Holding GmbH, Germany). Samples were prepared for shear testing on an aluminum oxide substrate and fixed by a thin layer of superglue (RS PRO 473-461, RS Components GmbH, Germany).

Figure 1: Transfer process overview for multiple microchips with active structures on top side (indicated by black line), simultaneously embedded into polyimide-based substrates with electrical interconnects. The black arrow points towards the top side of the carrier.

3 Results

The transfer process described previously was performed successfully and initial data about feasibility were gathered.

3.1 Transfer process

Chips were easily inserted into the cavities of the carrier wafer. These were designed to be slightly larger than the dice so as not to hinder the insertion process. However, they offered a tight fit for optimal alignment once the chips were set. It could be observed that the deposited sacrificial copper layer reached on the side walls of the cavities. Levelling the microchips and wafer back side by grinding led to no displacement of the former. Applying PI to the back side allowed problem-free removal of the UV-light-deactivated tape applied to the front side after exposure, without altering the chips' position. Figure 2 (i) shows a chip with its test structure inside a cavity, surrounded by the sacrificial copper layer. This allowed embedding the dice into PI on their front side. Thin-film metal interconnects could be fabricated by sputter deposition and lift-off technique. Via optical inspection, it was determined that all pads of the chips were in contact with the conductor paths. Figure 2 (ii) shows three chips located in the carrier wafer from the back side after grinding down to the desired thickness of 100 μm , which also did not result in any problems. Thus, transfer of the chips into PI was successful. Figure 3 shows one of the final devices incorporating three thinned dice ($390 \times 390 \mu\text{m}^2$, 100 μm thin) connected in series via the metal interconnects, after release from the carrier.

Figure 2: (i): Silicon die with metal structures placed in cavity of the carrier pictured from the top. Surrounding copper layer on the carrier serves as sacrificial layer for later release. (ii): Three silicon dice in cavities pictured from the back side after grinding them to the desired thickness of 100 μm .

Figure 3: Final sample after release with three embedded dice ($390 \times 390 \mu\text{m}^2$, 100 μm thin) connected in series by sputter deposited metal interconnects in flexible PI substrate. Sample held by tweezers and attached to micropipette for picture.

3.2 Yield analysis and mechanical characterization

With the process presented in this work, 100 % ($n = 34$) of the dice were transferred simultaneously into multiple PI substrates with a single structured Si-based carrier wafer. Embedded chip rotational error was determined to be as low as $0.21^\circ \pm 0.10^\circ$. Afterwards the samples were subject to mechanical examination by shear testing. Initial tests showed measured shear strength to be $58.1 \pm 13.7 \text{ MPa}$, which is comparable to chip transfer processes utilizing benzocyclobutene (BCB), an adhesive typically used for attachment [7, 8]. After accelerated ageing at elevated temperatures in a wet environment (16 days at 60°C in PBS), the average shear strength decreased to $15.2 \text{ MPa} \pm 10.5 \text{ MPa}$.

4 Discussion

The developed process allowed successful transfer of all 34 dice at once into PI substrates within this study. Here, their position in the carrier wafer was spaciouly chosen, hence even more chips could be transferred simultaneously, if desired. For this, the carrier would have to be provided with more cavities, accordingly. The position of the dice can be freely chosen in this process step. Cavities were designed in such a way that even during critical steps, such as removing the UV-light-deactivated adhesive tape, the position and orientation of the chips remained unaltered. This ensured contacting all the pads by metal interconnects with sufficient accuracy. This also shows that contact pads could be designed even smaller to more efficiently use available chip area.

Adhesion of the dice to the PI substrate reached values comparable to processes using BCB adhesive [7, 8]. The fact that PI accumulated between the individual chips and cavity sidewalls allows for the assumption that this contributed to overall adhesion strength by providing additional lateral support. Decrease in adhesion after accelerated ageing in wet environment might be attributed to swelling of the PI [9], as well as solution creeping between the substrate and chip in interstitial spaces.

Copper (Cu) was used as the sacrificial layer material as other materials typical for sacrificial layers (e.g. silicon dioxide (SiO₂) [10]) are used in later applications on different dice as functional layers. It would result in their dissolution and thus making them unusable after the release process. Subject of future experiments will be the investigation whether Cu residues remain on the PI surface and how the dice can be fully embedded for back side protection.

5 Conclusion

In this study, a novel scalable approach was presented to reliably transfer multiple microchips simultaneously into thin polyimide-based substrates with high accuracy. The use of a transfer wafer provided with dry etched cavities and a sacrificial layer resulted in very good alignment of test-chips. It allowed the use of microfabrication methods, such as photolithography and physical vapor deposition, for interconnect fabrication. Thinning of the dies during sample fabrication allows easier chip handling. As arbitrary chip sizes and positions are possible, the design can be adapted to fit different applications.

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