

Research article

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Experimental realization of an optical digital comparator using silicon microring resonators

<https://doi.org/10.1515/nanoph-2017-0073>

Received July 20, 2017; revised November 7, 2017; accepted November 29, 2017

Abstract: We propose and experimentally demonstrate a silicon photonic circuit that can perform the comparison operation of two-bit digital signals based on microring resonators (MRRs). Two binary electrical signals regarded as two operands of desired comparison digital signals are applied to three MRRs to modulate their resonances through the microheaters fabricated on the top of MRRs, respectively (here, one binary electrical signal is applied to two MRRs by a 1×2 electrical power splitter, which means that the two MRRs are modulated by the same binary electrical signal). The comparison results of two binary electrical signals can be obtained at two output ports in the form of light. The proposed device is fabricated on a silicon-on-insulator substrate using the complementary metal-oxide-semiconductor fabrication process, and the dynamic characterization of the device with the operation speed of 10 kbps is demonstrated successfully.

Keywords: directed logic; optical digital comparator; microring resonator; silicon photonic.

1 Introduction

Nowadays, academic communities, large semiconductor manufacturers, and startups are all competing to develop and commercialize high-performance silicon photonic

devices to resolve the problems faced by silicon electronic devices in the field of high-speed and large-capacity information processing, such as high power consumption, metal wire interconnect, and bandwidth limitation. Such a competitive situation mainly derives from the excellent performance of silicon photonic devices in information processing and their compatibility with complementary metal-oxide-semiconductor (CMOS) fabrication technology. Actually, more and more researchers believe that it is a promising choice to employ silicon photonic devices to replace silicon electronic devices in some specific aspects to resolve the problems faced by silicon electronic devices [1]. Various constituent components of a photonic information processing system fabricated by the CMOS-compatible fabrication process have already been demonstrated in experiments [2–8].

Being one of the basic components in the field of optical information processing, optical digital comparators are indispensable components for decision-making circuits, the integral part of arithmetic and logic units of optical data processors. Currently, most schemes for optical digital comparators are based on the nonlinearity of the material to achieve all-optical devices such as using semiconductor optical amplifiers [9, 10], Fabry-Pérot laser diodes [11], microring resonators (MRRs) [12], and plasmonic circuits [13]. However, all these schemes are fundamentally restricted to achieve large-scale integration, as a strong pump light is needed for these schemes to excite a nonlinear effect. To pursue low power consumption, large-scale integration, and low cost, integrated silicon photonic devices with the nature merits of compact size, low power, and compatibility with the standard commercial CMOS fabrication process are most desired. Although the integrated scheme for the digital comparator is also proposed and demonstrated [14], the structure of the device is complex, which includes two MRRs, one of them is with three coupling regions and one 1×2 power splitter. For MRR with three coupling regions, it is difficult to achieve the critical coupling to obtain better MRR performances.

In this paper, we report an alternative scheme to realize a two-bit digital comparator based on U-shaped

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waveguides and MRRs, which hold great potential for the construction of ultracompact, low-power, high-speed devices for next-generation silicon photonic circuits. The results of the comparator can be obtained at its two output ports simultaneously. The comparison operation is demonstrated successfully using a thermo-optic [15] effect. Compared to Ref. [14], our proposed structure of the device is simple, and the multimode interference (MMI) coupler and MRR with three coupling regions are eliminated in the integrated photonic circuit, which is very conducive to improve the signal quality and robust against the insertion loss of the device.

2 Device principle

The schematic of the proposed photonic circuit is shown in Figure 1, which consists of three MRRs (MRR_1 , MRR_2 , and MRR_3) connected by three U-shaped waveguides. Compared to Ref. [14], the proposed structure does not have three-coupling MRR and power splitter, which can improve the operation signal quality. The three ports of the circuit are defined as Input, Output C_1 , and Output C_2 according to their functions. The high and low levels of the electrical pulse sequences (EPS) applied to MRRs represent logic 1 and 0 in the electrical domain; the high and low levels of optical signals detected at output ports represent logic 1 and 0 in the optical domain. Monochromatic continuous-wave (CW) light at the working wavelength λ_w is coupled into the input of the device. Here, MRR_1 and MRR_3 are set as synchronous parts, which are modulated by EPS X simultaneously, whereas MRR_2 is modulated by another EPS Y. The MRR behaves as an optical switch in the proposed circuit: the working states of MRR can be controlled by applying voltage on the TiN microheater deposited on the top of MRR. When EPS X and Y are applied to the corresponding MRRs, the light signal coupled into the

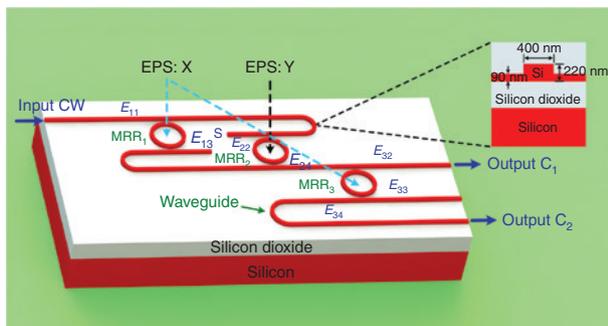


Figure 1: Schematic of the proposed digital comparator.

Input port can be directed to different propagation paths according to the applied high and low levels of EPS, as the effective refractive index of MRR is modulated through the thermo-optic effect. For example, when a high level is applied, the MRR is on-resonance at the working wavelength of λ_w , and the light signal coupled into the MRR is directed to the drop port; otherwise, the light signal is directed to the through port. To illuminate the principle of the circuit in detail, the four working states of all possible combinations are discussed as follows:

1. when $X=Y=0$ (the voltages applied to MRR_1 , MRR_3 , and MRR_2 are all at low level), all MRRs are off-resonance at the working wavelength of λ_w . The light signal coupled into the Input port of the circuit first bypasses MRR_1 , and then bypasses MRR_2 , finally directed to terminal S. As a result, the optical power obtained at Output ports C_1 and C_2 is both at low level, and logic 0 is achieved at two output ports ($C_1=0$, $C_2=0$);
2. when $X=0$ and $Y=1$ (the voltages applied to MRR_1 and MRR_3 are at low levels, whereas the voltage applied to MRR_2 is at high level). MRR_1 and MRR_3 are both off-resonance at the working wavelength of λ_w , whereas MRR_2 is on-resonance. The light signal coupled into the Input port of the circuit first bypasses MRR_1 and then downloaded by MRR_2 , subsequently bypasses MRR_3 , eventually directed to Output port C_1 . This means that logic 1 is achieved at Output port C_1 and logic 0 is achieved at Output port C_2 ($C_1=1$, $C_2=0$);
3. when $X=1$ and $Y=0$ (the voltages applied to MRR_1 and MRR_3 are at high levels, whereas the voltage applied to MRR_2 is at low level). MRR_1 and MRR_3 are on-resonance, whereas MRR_2 is off-resonance at the working wavelength of λ_w . The light signal coupled into the Input port of the circuit is first downloaded by MRR_1 , and then bypasses MRR_2 , subsequently downloaded by MRR_3 and directed to Output port C_2 . Consequently, logic 0 is achieved at Output port C_1 and logic 1 is achieved at Output port C_2 ($C_1=0$, $C_2=1$);
4. when $X=Y=1$ (the voltages applied to MRR_1 , MRR_3 , and MRR_2 are all at high levels), all the MRRs are on-resonance at the working wavelength of λ_w . The light signal coupled into the Input port of the circuit is downloaded by MRR_1 and MRR_2 successively and then directed to terminal S. Therefore, logic 0 can be achieved at Output ports C_1 and C_2 ($C_1=0$, $C_2=0$).

The logic truth table achieved by the proposed digital comparator in four working states are shown in Table 1, from which we can clearly see that, when $X=Y$ ($X=Y=0$ and $X=Y=1$), the combination output of C_1 and C_2 is $C_1C_2=00$; when $X < Y$ ($X=0$, $Y=1$), the combination output

Table 1: Logic truth table achieved by the proposed digital comparator.

X	Y	Output C ₁		Output C ₂		Comparison results C ₁ C ₂ combinations
		Power level	Logic	Power level	Logic	
0	0	Low	0	Low	0	00 (X=Y)
0	1	High	1	Low	0	10 (X<Y)
1	0	Low	0	High	1	01 (X>Y)
1	1	Low	0	Low	0	00 (X=Y)

of C₁ and C₂ is C₁C₂=10; and when X>Y (X=1, Y=0), the combination output of C₁C₂=01. Obviously, the circuit can perform the comparing function of two-bit binary electrical signals, and the operation results are obtained at output ports in the form of light.

The performance of the device can be derived based on the scattering matrix model [16]. The relationship between the input and output electric fields can be derived as follows:

$$\begin{bmatrix} E_{32} \\ E_{34} \end{bmatrix} = \begin{bmatrix} T_3 & D_3 \\ D_3 & T_3 \end{bmatrix} \times \begin{bmatrix} Q_3 & 0 \\ 0 & 1 \end{bmatrix} \times \begin{bmatrix} E_{24} \\ E_{33} \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} E_{24} \\ E_{22} \end{bmatrix} = \begin{bmatrix} T_2 & D_2 \\ D_2 & T_2 \end{bmatrix} \times \begin{bmatrix} Q_2 & 0 \\ 0 & Q_1 \end{bmatrix} \times \begin{bmatrix} D_1 & T_1 \\ T_1 & D_1 \end{bmatrix} \times \begin{bmatrix} E_{11} \\ E_{13} \end{bmatrix} \quad (2)$$

where E_{11} , E_{13} , E_{22} , E_{24} , E_{32} , E_{33} , and E_{34} are the amplitudes of the electric fields in the corresponding ports of the MRRs (shown in Figure 1), respectively. The light is only input from the Input port of the device; therefore, Eqs. (1) and (2) can be simplified and rewritten as

$$E_{32} = T_3 Q_3 \times (T_2 Q_2 D_1 + D_2 Q_1 T_1) \times E_{11} \quad (3)$$

$$E_{34} = D_3 Q_3 \times (T_2 Q_2 D_1 + D_2 Q_1 T_1) \times E_{11} \quad (4)$$

where

$$T_m = \frac{t_m - t_m \alpha_m \exp(j\Phi_m)}{1 - \alpha_m t_m^2 \exp(j\Phi_m)} \quad (5)$$

$$D_m = \frac{-\alpha_m^{1/2} k_m^2 \exp(j\Phi_m / 2)}{1 - \alpha_m t_m^2 \exp(j\Phi_m)} \quad (6)$$

$$\Phi_m = \theta_m + \Delta\theta_m = 4\pi^2 (n_{\text{eff}} + \Delta n_{R_m\text{-eff}}) \times R_m / \lambda \quad (7)$$

$$Q_m = \alpha_{L_m} \times \exp(j\varphi_m) \quad (8)$$

$$\varphi_m = 2\pi n_{\text{eff}} L_m / \lambda \quad (9)$$

Among them, $m=1, 2$, and 3 . t_m , k_m , α_m , and R_m are the transmission coefficient, coupling coefficient, amplitude transmission factor, and radius of the m th MRR, respectively. L_m and α_{L_m} are the length and amplitude transmission factor of the waveguides between the MRRs, respectively. n_{eff} and $\Delta n_{R_m\text{-eff}}$ are the effective refractive index of the ridge waveguide (Figure 1, inset) and its variations in the MRRs. λ is the optical wavelength.

3 Fabrication and experimental result

The proposed device is fabricated on silicon-on-insulator substrate with 220-nm-thick top silicon layer and 2- μm -thick buried SiO₂ layer using the standard CMOS fabrication process (Figure 2). A 248-nm-deep ultraviolet lithography technology is employed to define the pattern of the device, and inductively coupled plasma dry etching is employed to etch the top silicon layer. After forming the top silicon waveguide pattern, a 2- μm -thick SiO₂ layer is deposited on the top of silicon waveguide regarded as the isolation layer between optical and electrical signals. Then, TiN microheaters with width of 2 μm and thickness of 120 nm are fabricated on the top of ring waveguides to modulate MRRs through a thermo-optic effect. Aluminum traces are formed to connect the microheaters and the 100 \times 100 μm^2 pads at last. To enhance the coupling efficiency, a 200- μm -long linearly inversed taper with a 180-nm-wide tip regarded as spot size converter (Figure 2B) is integrated on the input and output terminals of the device, respectively [17]. The effective area of the device is about 100 \times 450 μm^2 .

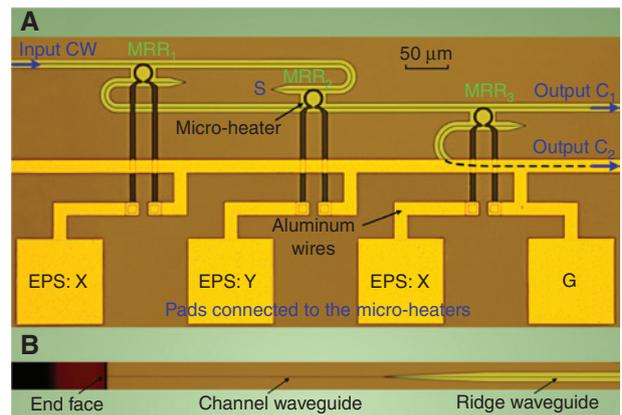


Figure 2: The proposed device is fabricated based on the CMOS process: (A) is the micrograph of the fabricated device and (B) is the micrograph of the spot size converter.

As we know, the CMOS fabrication process has limited accuracy, which would mainly have impacts on the performance of the proposed device. The one impact is on the radii of the MRRs, which will lead to different resonant wavelengths of each MRR. However, this could be overcome by applying different high-level voltages to tune the MRR to the working wavelength. The other impact is on the gaps between the MRRs and straight waveguides, which will lead to different extinction ratios of each MRR. The proposed device is fabricated using a commercial CMOS fabrication process at the Institute of Microelectronics in Singapore. From the experimental results in Figures 3B and 4C, we can see that the three MRRs have almost equal extinction ratios. Therefore, the fabrication error is relatively small in the gaps of the MRRs based on the CMOS fabrication process in the state of art.

To determine the working wavelength λ_w and the working voltages of the device, the static response spectra under different working states are characterized first. A broadband amplified spontaneous emission (ASE) source, three tunable voltage sources, and an optical spectrum analyzer (OSA) are employed to characterize

the static response spectra of the device. The broadband light from ASE is coupled into the Input port of the device through a lensed fiber, and the output light signal is fed into the OSA through another lensed fiber. In fact, all wavelengths longer than 1544.00 nm in a free spectral range could be chosen as the working wavelength. However, too short wavelength will lead to small extinction ratio between logic 0 and 1, and too long wavelength will lead to large input electrical power as well as long response time. We chose the working wavelength at λ_w of 1544.32 nm to achieve relative high extinction ratio and low power consumption. The static response spectra of the device at Output port C_1 are shown in Figure 3A–D, and the static response spectra at Output port C_2 are shown in Figure 4A–D, respectively.

Theoretically, the three MRRs should have the same resonant wavelength, as they are designed to have the same physical parameters; however, they have different resonances for the fabricated device due to the limited fabrication accuracy. To make all MRRs have the same resonant wavelength at their initial states and reduce the fluctuation of low level for different logic 0s in dynamic

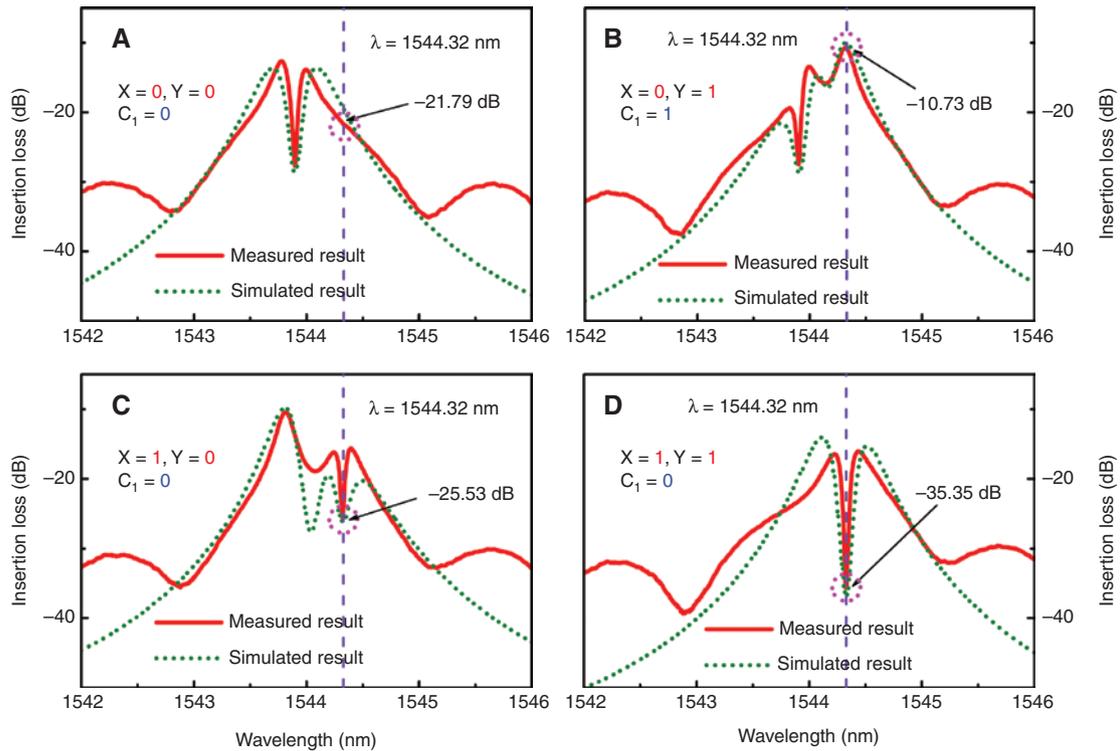


Figure 3: Measured and simulated response spectra of the device at Output port C_1 with the additional voltages applied to MRR_1 , MRR_2 , and MRR_3 and the corresponding effective refractive index variations: (A) $\Delta V_1 = \Delta V_2 = \Delta V_3 = 0.00$ V and $\Delta n_{R1\text{-eff}} = \Delta n_{R2\text{-eff}} = \Delta n_{R3\text{-eff}} = 0$; (B) $\Delta V_1 = \Delta V_3 = 0.00$ V, $\Delta V_2 = 0.46$ V, $\Delta n_{R1\text{-eff}} = \Delta n_{R3\text{-eff}} = 0$, $\Delta n_{R2\text{-eff}} = 8.8 \times 10^{-4}$; (C) $\Delta V_1 = 0.58$ V, $\Delta V_2 = 0.00$ V, $\Delta V_3 = 0.50$ V, $\Delta n_{R1\text{-eff}} = 12.0 \times 10^{-4}$, $\Delta n_{R2\text{-eff}} = 0 \times 10^{-4}$, $\Delta n_{R3\text{-eff}} = 10.2 \times 10^{-4}$; and (D) $\Delta V_1 = 0.58$ V, $\Delta V_2 = 0.46$ V, $\Delta V_3 = 0.50$ V, $\Delta n_{R1\text{-eff}} = 12.0 \times 10^{-4}$, $\Delta n_{R2\text{-eff}} = 8.8 \times 10^{-4}$, $\Delta n_{R3\text{-eff}} = 10.2 \times 10^{-4}$, respectively.

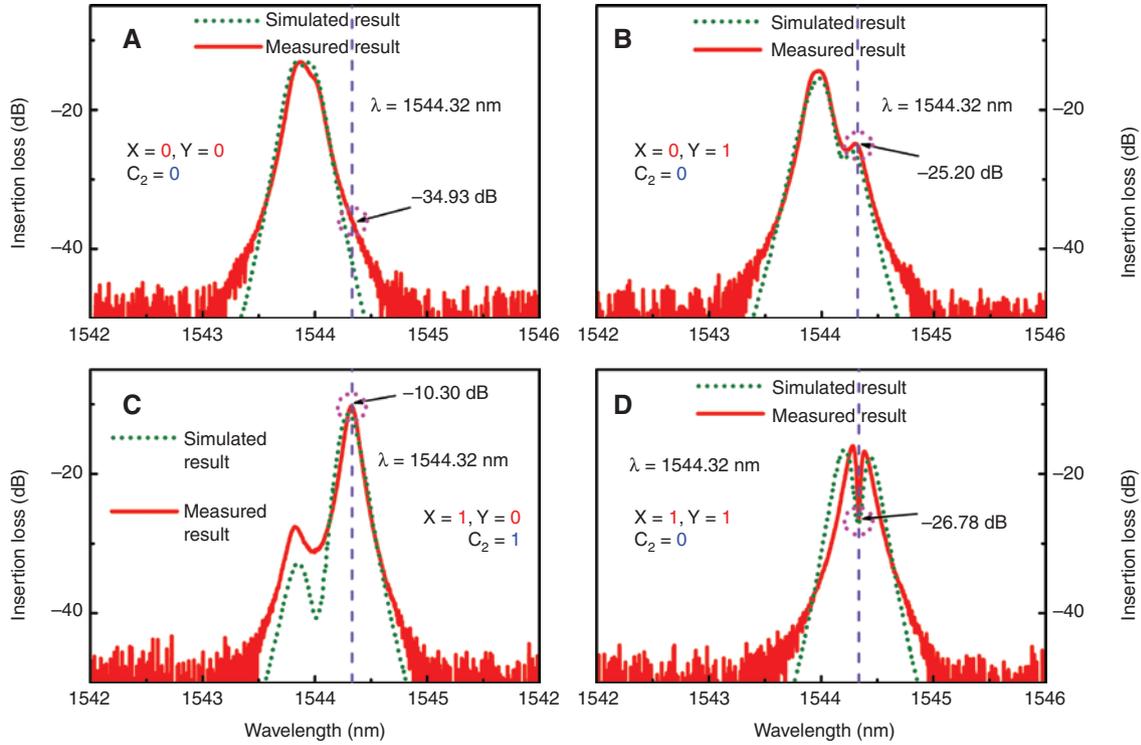


Figure 4: Measured and simulated response spectra of the device at Output port C_2 with the additional voltages applied to MRR_1 , MRR_2 , and MRR_3 and the corresponding effective refractive index variations: (A) $\Delta V_1 = \Delta V_2 = \Delta V_3 = 0.00$ V and $\Delta n_{R1\text{-eff}} = \Delta n_{R2\text{-eff}} = \Delta n_{R3\text{-eff}} = 0$; (B) $\Delta V_1 = \Delta V_3 = 0.00$ V, $\Delta V_2 = 0.46$ V, $\Delta n_{R1\text{-eff}} = \Delta n_{R3\text{-eff}} = 0$, $\Delta n_{R2\text{-eff}} = 8.8 \times 10^{-4}$; (C) $\Delta V_1 = 0.58$ V, $\Delta V_2 = 0.00$ V, $\Delta V_3 = 0.50$ V, $\Delta n_{R1\text{-eff}} = 12.0 \times 10^{-4}$, $\Delta n_{R2\text{-eff}} = 0 \times 10^{-4}$, $\Delta n_{R3\text{-eff}} = 10.2 \times 10^{-4}$; and (D) $\Delta V_1 = 0.58$ V, $\Delta V_2 = 0.46$ V, $\Delta V_3 = 0.50$ V, $\Delta n_{R1\text{-eff}} = 12.0 \times 10^{-4}$, $\Delta n_{R2\text{-eff}} = 8.8 \times 10^{-4}$, $\Delta n_{R3\text{-eff}} = 10.2 \times 10^{-4}$, respectively.

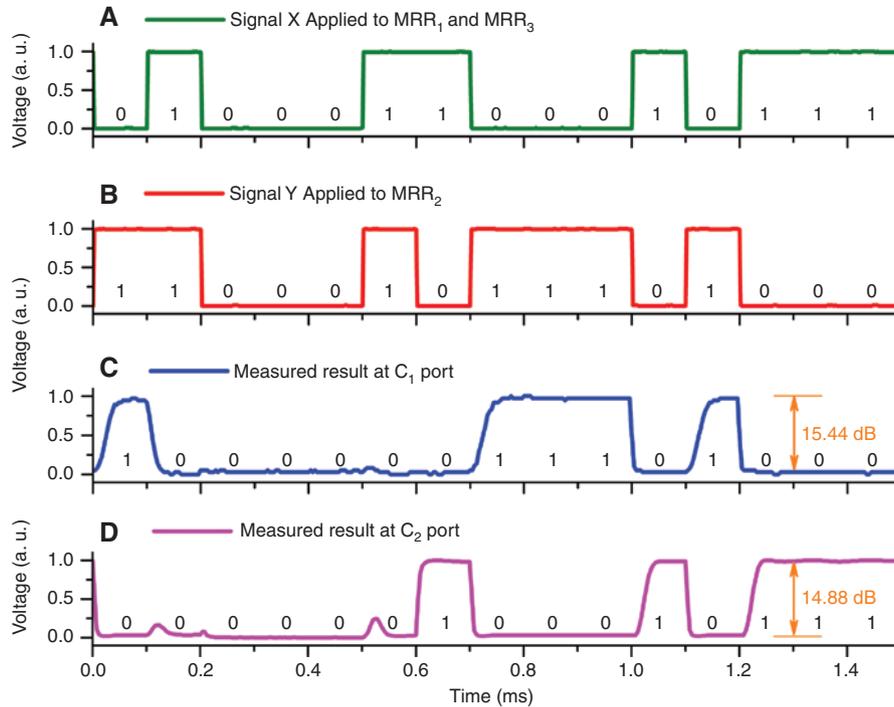
measurement, prebias voltages of 2.23 and 1.63 V are applied to MRR_1 and MRR_2 , respectively. The static response spectrum at port C_1 with no additional voltages ($X=Y=0$) applied to the three MRRs is shown in Figure 3A. When the additional voltage of $\Delta V_2 = 0.46$ V is applied to MRR_2 and the additional voltages applied to MRR_1 and MRR_3 are both 0.00 V, the resonant wavelength of MRR_2 will shift to the working wavelength λ_w of 1544.32 nm, and the resonant wavelengths for MRR_1 and MRR_3 are unchanged ($X=0$, $Y=1$). Therefore, there is a resonant peak at the working wavelength of 1544.32 nm, which represents the drop filtering characteristics of MRR_2 (Figure 3B). When the additional voltages applied to MRR_1 and MRR_3 are $\Delta V_1 = 0.58$ V and $\Delta V_3 = 0.50$ V, respectively, whereas the additional voltage applied to MRR_2 is $\Delta V_2 = 0.00$ V, the resonant wavelengths for MRR_1 and MRR_3 are both shifted to the working wavelength of 1544.32 nm ($X=1$, $Y=0$). Hence, in Figure 3C, we can see the superposition of a dip and a peak at the working wavelength of 1544.32 nm, which represents the combination characteristic of the through filtering of MRR_3 and the drop filtering of MRR_1 . When the additional voltages applied to MRR_1 , MRR_2 , and MRR_3 are $\Delta V_1 = 0.58$ V, $\Delta V_2 = 0.46$ V, and $\Delta V_3 = 0.50$ V, respectively,

their resonant wavelengths are all shifted to the working wavelength of 1544.32 nm ($X=1$, $Y=1$). There is a superposition of a resonant peak and two resonant dips at the working wavelength of 1544.32 nm, which represents the combination characteristic of the drop filtering of MRR_1 , the through filtering of MRR_2 , and the through filtering of MRR_3 (Figure 3D). Similar analyses are also effective for Figure 4, which is not discussed here due to the limitation of text content. The simulated performances of the device based on Eqs. (1–9) are also shown in Figures 3 and 4 with green dotted lines, from which we can clearly see that the theoretical model can commendably predict the performance of the device. The small ripples on both sides of the resonant wavelength in the measured results are mainly due to the reflection of the terminal ports.

In Figures 3 and 4, we can see clearly that the insertion losses at the working wavelength λ_w for different working states are different. In other words, the optical power output at Output ports C_1 and C_2 at the working wavelength of 1544.32 nm is different in different working states, which also represents different logic value. The insertion losses, optical power, and logic values at the working wavelength in different working states are summarized as Table 2,

Table 2: Insertion loss, optical power, and logic values at the working wavelength in different working states.

EPS		Output C_1			Output C_2		
X	Y	Insertion loss (dB)	Power level	Logic	Insertion loss (dB)	Power level	Logic
0	0	-21.79	Low	0	-34.93	Low	0
0	1	-10.73	High	1	-25.20	Low	0
1	0	-25.53	Low	0	-10.30	High	1
1	1	-35.35	Low	0	-26.78	Low	0

**Figure 5:** The dynamic performances of the device are measured. (A) is the electrical signals applied to MRR₁ and MRR₃, (B) is the electrical signal applied to MRR₂, (C) and (D) are the comparison results at C₁ and C₂ ports respectively.

from which we can see that the proposed device can perform the comparison operation of two-bit binary logic signals, and the comparison operation result is obtained at Output ports C₁ and C₂ in the form of light. For example, when $X > Y$, the comparison operation result is 01 ($C_1 = 0$, $C_2 = 1$); when $X < Y$, the comparison operation result is 10 ($C_1 = 1$, $C_2 = 0$); and when $X = Y$, the comparison operation result is 00 ($C_1 = 0$, $C_2 = 0$). Note that, in defining the logics of the optical output results, threshold levels are adopted to distinguish logic 1 and 0 [6, 18].

The dynamic response performance of the device is also characterized with a tunable laser (TL), arbitrary function generator (AFG), a four-channel oscilloscope (OSC), and a photodetector (PD).

Monochromatic CW light generated by a TL with the wavelength of 1544.32 nm is first coupled into a polarization controller, and then the light with TE polarization is

coupled into the Input port of the device through a lensed fiber. Three 15-bit NRZ-coded pseudo-random binary sequences (PRBS) at the speed of 10 kbps generated by the AFG with appropriate amplitudes and offsets are applied to MRR₁, MRR₂, and MRR₃ through the microheaters fabricated on the top of them, respectively. Note that two of the three PRBS signals are the same and synchronous (regarded as X, but they are with different high levels due to the different parameters caused by the limited fabrication accuracy), and they are applied to MRR₁ and MRR₃, as MRR₁ and MRR₃ are regarded as synchronous parts. Therefore, the working states of MRR₁ and MRR₃ are controlled by logic operand X. The working state of MRR₂ is controlled by the logic operand Y. The output optical signal at the output port of the device is fed into a PD through another lensed fiber. The electrical signal output from the PD is fed into the OSC for waveform observation. The dynamic

response result of the fabricated device is shown in Figure 5, which indicates that the fabricated device can achieve the comparison operation of two-bit digital signals correctly. The maximum rising and falling times are about 22 and 15 μs for the operation result obtained at Output C_1 port and about 15 and 7 μs for Output C_2 port, respectively. The minimum extinction ratios are 15.44 and 14.88 dB for the operation results obtained at Output C_1 and C_2 ports, respectively. Compared to Ref. [14], the structure of the proposed device is relatively simpler (MMI coupler and multicoupling region are eliminated in the structure of the device), and the quality of the dynamic signal that does not have a secondary high level in logic 1 is better. Compared to other high-speed modulation mechanisms that usually have complex fabrication processes and high costs [11, 19, 20], the thermo-optic effect is more suitable for the proof-of-concept due to its simple fabrication process. Our next research target is to employ the electro-optic effect of PIN- and PN-based MRR to implement higher working speed to meet the requirements of future applications.

4 Conclusion

In conclusion, we have proposed and demonstrated an integrated photonic circuit that can perform the comparison operation of two-bit digital signals based on cascaded thermo-optic tunable MRRs. Finally, the dynamic characterization of the device with the operation speed of 10 kbps was demonstrated successfully.

Acknowledgments: This work was supported in part by the National Science Foundation of China (Grant 61405082), Fundamental Research Funds for the Central Universities (Grant lzujbky-2016-k05), Open Project of Key Laboratory for Magnetism and Magnetic Materials of the Ministry of Education (LZUMMM2017005), and Opened Fund of the State Key Laboratory on Integrated Optoelectronics (IOSKL2016KF14).

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