Research article

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Temperature-stable black phosphorus field-effect transistors through effective phonon scattering suppression on atomic layer deposited aluminum nitride

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Abstract: Black phosphorus (BP) shows great potential in electronic and optoelectronic applications; however, maintaining the stable performance of BP devices over temperature is still challenging. Here, a novel BP field-effect transistor (FET) fabricated on the atomic layer deposited AlN/SiO_2/Si substrate is demonstrated. Electrical measurement results show that BP FETs on the AlN substrate possess superior electrical performance compared with those fabricated on the conventional SiO_2/Si substrate. It exhibits a large on-off current ratio of 5×10^8, a low subthreshold swing of <0.26 V/dec, and a high normalized field-effect carrier mobility of 1071 $cm^2\ V^{-1}\ s^{-1}$ in the temperature range from 77 to 400 K. However, these stable electrical performances are not found in the BP FETs on SiO_2/Si substrate when the temperature increases up to 400 K; instead, the electrical performance of BP FETs on the SiO_2/Si substrate degrades drastically. Furthermore, to gain a physical understanding on the stable performance of BP FETs on the AlN substrate, low-frequency noise analysis was performed, and it revealed that the AlN film plays a significant role in suppressing the lattice scattering and charge trapping effects at high temperatures.

Keywords: black phosphorus; atomic layer deposition; field-effect transistor; low-frequency noise; interface state.

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1 Introduction

Two-dimensional materials such as graphene and transition metal dichalcogenides have been considered as promising candidates for next-generation electronic devices [1–8]. Graphene has an extremely high carrier mobility; however, its application on low power consumption circuits is severely limited because of the absence of an intrinsic energy bandgap [1–3]. On the other side, transition metal dichalcogenides based field-effect transistors (FETs) with moderate bandgap (e.g. MoS_2, WSe_2, and WS_2) always suffer from a low field-effect mobility because of the imperfection of source/drain metal contacts [4–6]. Recently, black phosphorus (BP) has attracted intensive interests because of its unique physical and electrical properties. BP is the most stable allotrope of phosphorus, and unlike graphene, it has a direct bandgap varying from 0.3 eV for bulk to 1.8 eV for monolayer [7]. Currently, typical BP FETs show a high carrier mobility of up to 1000 $cm^2\ V^{-1}\ s^{-1}$, an on/off current ratio larger than 10^5, showing their great potential for future applications in electronic and optoelectronic devices [7–21].

Nevertheless, BP reacts easily with water and oxygen; thus, the performance and stability of BP FETs are significantly affected by the ambient conditions [22]. At present, several approaches have been proposed to improve the BP stability against water and oxygen, such as covering BP by stacking *h*-BN [23], capping Al_2O_3 [24–27], atomistic fluorination [28], ligand surface coordination [29, 30], and covalent aryl diazonium functionalization [31]. However, the interface property between the BP and gate oxide attracts less attention, although it is also one of the critical factors limiting the device performance and stability.

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Theoretically, the intrinsic hole mobility of the few-layer BP at room temperature can exceed 5000 $cm^2 V^{-1} s^{-1}$, and the intrinsic electron mobility can also reach 1000 $cm^2 V^{-1} s^{-1}$ [32], although the field-effect mobility achieved in practical was far less than its theoretical prediction. Similar observations are also reported in other two-dimensional materials [33–40]. Currently, the understanding of these mobility degradations is that the carriers' motion is constrained in the atomic-layer thickness region, which is more easily affected by the surface condition than that of bulk materials. Therefore, it is necessary to explore a better interface to solve this critical problem that affects the electrical performance and application of BP FETs.

Up to now, Coulomb scattering and lattice scattering are considered as two major factors that weaken the carrier transport and field-effect mobility [33–35, 41]. Therefore, to mitigate the carrier mobility degradation, one approach is to improve the interface quality, which can be achieved by reducing the impurities and interface defects between channel material and dielectric layer. In the meanwhile, improved material and dielectric layer are also helpful to alleviate the impact of lattice scattering by choosing substrate or capping layer materials with higher surface phonon energy. In previous studies, the high surface phonon energy material such as hexagonal boron nitride (*h*-BN), which has the surface phonon energy of 101 meV [35], was regarded as the ideal substrate for many two-dimensional materials. However, the preparation of high-quality and wafer-scale *h*-BN is highly challenging. Other materials with high surface phonon energy such as the diamond-like carbon and SiC, whose surface phonon energy exceeds 100 meV, were also limited by the high cost and immature preparation technology. While aluminum nitride (AlN) owns a higher surface phonon energy than conventional substrates such as SiO_2 and Al_2O_3 [33, 35], it can be grown by atomic layer deposition or sputtering in a wafer scale, which is highly compatible with the existing main stream process [33, 42–46]. All these merits put AlN to be an attractive substrate for high-performance BP electronics.

Low-frequency noise (LFN) is a significant index to evaluate the device performance, and it is critical to gain the underlying mechanism of the LFN characteristic in achieving highly sensitive and stable devices. Na et al. investigated the charge transport characteristic of BP FETs before and after Al_2O_3 passivation by measuring the $1/f$ noise, the carrier fluctuation model related to the charge trapping/detrapping process was applied to explain the LFN behavior of the n- and p-branches of the BP devices [47–50]. In this work, we fabricated BP FETs on AlN/SiO_2/Si substrates, thereafter the electrical characteristic under different temperatures was characterized to evaluate its interface property and stability. To explore the underlying mechanism of excellent stability of BP FETs on AlN substrates, low-frequency noise was performed to examine the dominant current noise fluctuations. Moreover, the interfacial charge densities as a function of temperature are also evaluated quantitatively for comparison of two different interfaces.

2 Experimental section

Heavily doped p-type silicon wafers (resistivity <0.005 Ω cm) with 285 nm thermal oxide were used as the conventional SiO_2/Si substrate, and the AlN thin-film was grown on the SiO_2/Si substrate by atomic layer deposition (ALD, Beneq TFS200) at 200°C using Beneq TFS200. Few-layer BP flakes were mechanically exfoliated from bulk BP (purity = 99.998%, Smart Elements) and transferred onto the substrate using polydimethylsiloxane for fewer residuum. Then, the poly methyl methacrylate was spin-coated as e-beam lithography (EBL, 6300FS, JEOL) photoresist for the definition of source and drain contacts, and electrodes of Ni (20 nm)/Au (80 nm) were formed using e-beam evaporation and followed by a lift-off process. A 30 nm ALD Al_2O_3 passivation was capped on the backside of the BP channel to form the isolation between BP and air ambient. No annealing process was performed. The roughness of AlN films and thickness of BP were measured by atomic force microscopy (AFM, Bruker Icon). The composition measurement of AlN films was performed with X-ray photoelectron spectroscopy (XPS, AXIS Ultra DLD, Shimadzu). The electrical characteristics of BP FETs at low temperatures were measured on a semiconductor parameter analyzer (Keysight B1500A) with a cryogenic probe station in vacuum. Low-frequency noise measurements were carried out using Industry's Fast $1/f$ Noise System (PDA NC300A). Raman spectroscopy measurements were performed using LabRAM HR800 (Horiba Jobin Yvon) with an excitation wavelength of 532 nm at room temperature in the ambient air, where the Raman spectral resolution was 1.1 cm^{-1}.

3 Results and discussion

Figure 1A–D show the optical and AFM images of BP FETs fabricated on bare SiO_2(285 nm)/Si and AlN(10 nm)/SiO_2(285 nm)/Si substrates (henceforth named Device S and Device A, respectively). The structures of the

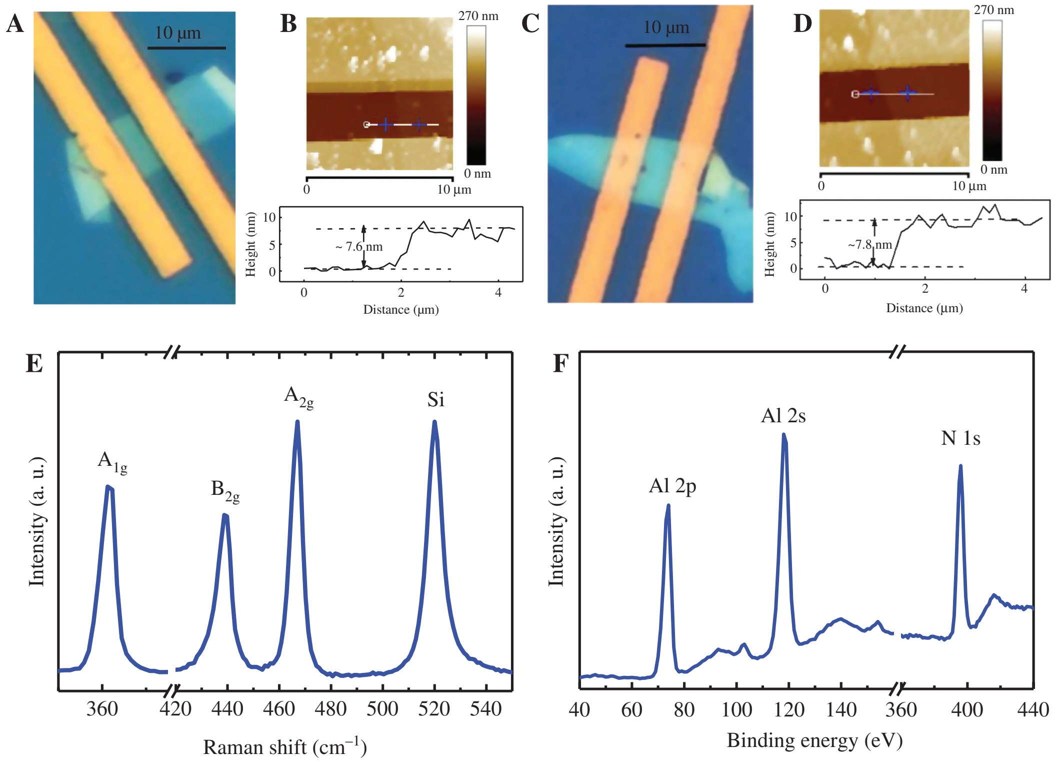

Figure 1: The AFM, Raman and XPS characterizations of the fabricated BP devices.
Optical microscope image of fabricated devices on (A) AlN/SiO_2/Si and (C) SiO_2/Si substrates. Atomic force microscope (AFM) image and the extracted thickness of BP channel for devices on (B) AlN/SiO_2/Si and (D) SiO_2/Si substrates. (E) Raman spectrum of few-layer black phosphorus as exfoliated; one out-of-plane mode (A_{1g}) and two in-plane modes (A_{2g} and B_{2g}) of few-layer BP can be clearly observed. (F) XPS of atomic-layer-deposited AlN film.

aforementioned BP devices are schematically illustrated in Figure S1. The extracted BP channel thicknesses of both devices are comparable, i.e. 7.8 nm for Device S and 7.6 nm for Device A, which were confirmed by AFM. The gate capacitance of the hybrid substrate is roughly 1.3% smaller than that of the SiO_2 substrate; hence, the impact on the carrier density modulated electrostatically by a given gate bias can be negligible. In addition, the AFM measurements of the two substrates also exhibit comparable surface roughness, as shown in Figure S1, indicating an excellent uniformity of the AlN film. This is important to eliminate the effect of surface roughness on the electrical characteristic. Figure 1E shows the Raman spectrum of as-exfoliated few-layer BP, which is consistent with previous observations [51–53]. The XPS analysis of AlN substrate (Figure 1F) obtained spectrum peaks of Al 2*p* at 73.9 eV and N 1*s* at 397.0 eV, corresponding to the Al-N bonds [54]. The atomic ratio of Al/N elements is 1.2, calculated with peak area divided by relative sensitivity factors, which is close to the chemical stoichiometric of AlN. A 30 nm Al_2O_3 film was capped, via ALD, at the backside of the BP channel for two reasons: (i) to protect the BP FETs from degradation caused by O_2 and H_2O in the ambient, and (ii) to isolate the charge trapping from the surroundings.

To figure out the difference between Device S and Device A, electrical measurement was carried out against temperature. It is shown that both BP FETs exhibited excellent performance in the low-temperature region, i.e. a high on-current (I_{on}) of 1 μA/μm, a low off-current (I_{off}) of 5.13×10^{-10} μA/μm, and a high on/off current ratio over 1.3×10^{9}. Additionally, a very small subthreshold swing (SS) of less than 0.26 V/dec was observed, surpassing most of BP FETs ever reported [5–7, 55]. As it can be seen in Figure 2A and B, both devices exhibited ambipolar transport characteristics. Compared with Device S, Device A showed a weaker n-type transport under all temperatures, and the maximum current of p-type conduction was 4 orders of magnitude larger than that of n-type at 77 K. Device S, however, showed the same order of maximum current in both n- and p-type conduction. As the temperature increases, the current minimum of Device A shifts toward the more positive bias region, implying that its p-type conduction is prone to be deteriorated. It appears that the AlN substrate facilitates the transport of holes, and thus, it is suitable for the realization of unipolar FETs.

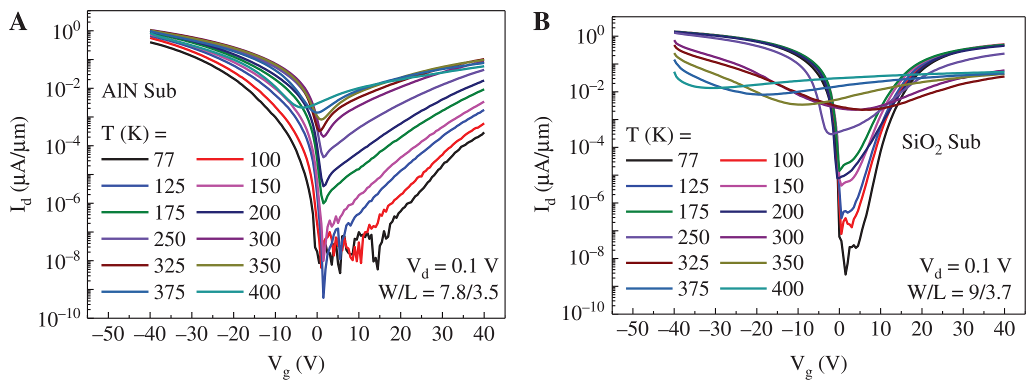

Figure 2: Temperature dependent electrical characteristics of BP FETs on two substrates.
I_d-V_g characteristics as a function of temperature from 77 to 400 K for BP FETs on (A) AlN/SiO$_2$/Si and (B) bare SiO$_2$/Si substrates.

A drastic degradation in electrical performance of Device S is observed in the high-temperature region of over 250 K. The I_{on} of Device S decreases by 30 times with the temperature increasing from 77 to 400 K (~0.05 μA/μm), thus reducing the on/off current ratio from 5×10^8 to less than 5, as shown in Figure 3A and C. In contrast, the I_{on} of Device A remains quite stable up to a high temperature of 400 K (~1 μA/μm). Meanwhile, Device A also exhibits a consistently lower I_{off} in the entire temperature range, compared with Device S, as plotted in Figure 3B. The on/off current ratio of Device A at 400 K is larger than 400, approximately a hundred times larger than that of Device S. Moreover, the SS of Device A shows a better performance with respect to Device S, as shown in Figure 3D. It is observed that the SS of the latter increases to 27.6 V/dec at 400 K, which is 150 times of the smallest value at 77 K.

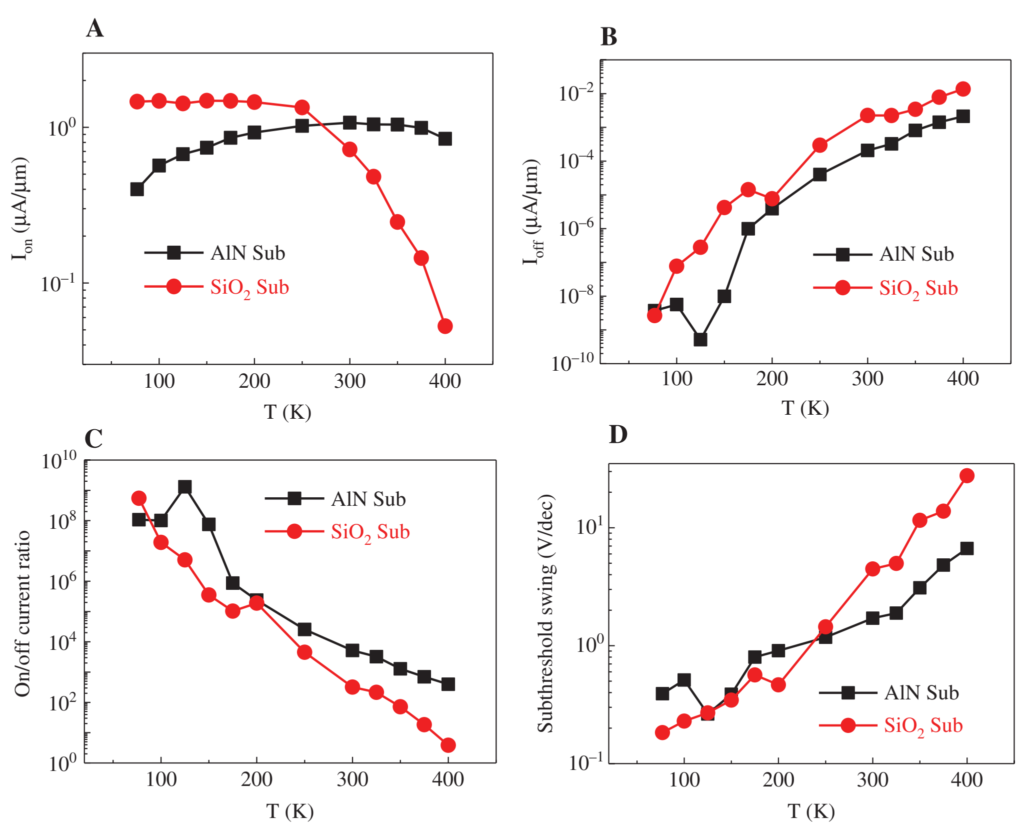

Figure 3: The device parameters for BP FETs as a function of temperature.
Temperature evolution of (A) on currents, (B) off currents, (C) on-off current ratio, and (D) subthreshold swing of BP FETs on different substrates extracted from I_d-V_g curves.

However, the temperature dependence of mobility remains largely unchanged except for the slope at high temperatures. Therefore, the drastic difference between Device S and Device A is mainly due to the charge traps, which introduce an exponential term with temperature due to the thermal excitation of carriers to the conduction band.

Figure 4 depicts the field-effect mobility (μ_{FE}) of two types of devices as a function of temperature ranging from 77 to 400 K. Contact resistance is calculated and decoupled from the total resistance [56], assuming that the channels were fully conducting at high V_{gs}. The μ_{FE} of BP FETs can be estimated by using the following equation [6, 7, 27]: $\mu_{FE} = \dfrac{g_m L}{W C_{ox} V_{ds}}$, where L and W represent the channel length and width, respectively. The transconductance (g_m) equals to $\Delta I_{ds}/\Delta V_{gs}$, C_{ox} is 11.95 nF/cm² for the AlN/SiO_2 and 12.11 nF/cm² for the bare SiO_2. At 77 K, the highest μ_{FE} observed for hybrid and bare SiO_2 substrates are 1071 and 721 cm² V⁻¹ s⁻¹, respectively. Presently, it is believed that the mobility can be limited by Coulomb impurities (CI) scattering, lattice scattering, charge traps, and defects, which is similar to that of other two-dimensional materials [33, 34, 57]. At temperature below 120 K, CI scattering plays the dominant role in limiting the mobility of BP FETs, whereas at high temperature above 120 K, the surface phonon (or lattice scattering) dominates [41]. The mobility of both BP FETs degrades with increasing temperature; in particular, Device S suffers a pronounced mobility degradation of nearly 2 orders of magnitude at high temperatures. In contrast, Device A shows only less than 1 order of magnitude in degradation. The mobility was suppressed because of phonon scattering, which limits the holes transport accordingly by $\mu_{FE} \sim T^{-\theta}$, where the exponent θ depends on the dominant scattering mechanism. The dashed lines were fitted according to $\mu_{FE} \sim T^{-\theta}$, where $\theta = 0.2 \sim 0.3$ at low temperatures (77–250 K) and increases rapidly at high temperatures, suggesting that the phonon scattering between carriers and lattice intensifies with increasing temperature. The θ of Device A is smaller than that of Device S, signifying a modest scattering intensity at the interface between AlN and BP. The intense scattering between carriers and lattice under the high temperature severely degrades the mobility. Note that the irreversible degradation of device performance can be negligible at high temperature, which can be seen in Figure S2. Considering AlN film's properties with high dielectric constant of 9.14 and surface phonon energy of 83.6 meV, which is relatively larger than that of SiO_2 (3.9 and 59 meV) [33, 35], the much higher carrier mobility of Device A at high temperatures could be attributed to the high surface phonon energy and less charge traps and defects in the AlN film [33, 43].

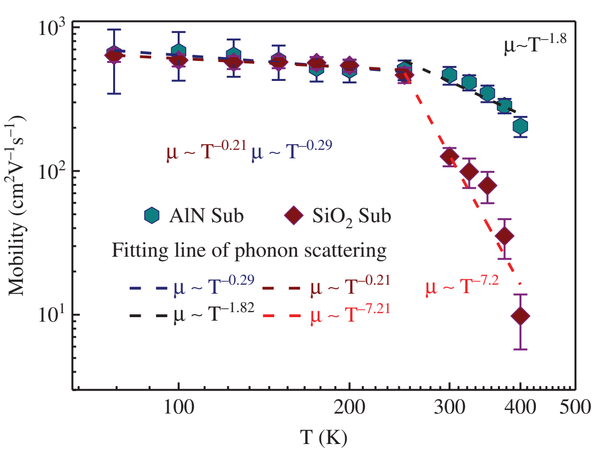

Figure 4: Field-effect mobility (μ_{FE}) of BP FETs on AlN/SiO_2/Si and SiO_2/Si substrates as a function of temperature. The mobility was suppressed because of phonon scattering limited transport, which follows $\mu_{FE} \sim T^{-\theta}$, where the exponent depends on the dominant scattering mechanism. The dashed lines are fitting results according to this law, where the θ is about $0.2 \sim 0.3$ at low temperatures within 77–250 K and increases rapidly at high temperatures, indicating the intense phonon scattering between carriers and lattice. The θ for BP FETs on the AlN substrate is much smaller than that on the SiO_2 substrate, suggesting a modest scattering intensity at the interface between AlN and BP.

We further implemented the LFN measurements for two types of devices at high temperatures above 300 K. LFN, also known as $1/f$ noise, is a significant way to measure a device's performance, particularly for its interface properties. The power spectral density of the current noise S_I for $1/f$ noise takes a general form as follows [58]:

$$S_I = \frac{K I^{\beta}}{f^{\gamma}} \tag{1}$$

where K is a constant value, β is a current exponent of ~2, and S_I is proportional to $1/f^{\gamma}$ with γ ranging from 0.7 to 1.3 [58]. The transfer characteristics of these two devices are shown in Figure S3. Figure S4 shows the LFN characteristic of Device A and Device S under various gate voltage ranging from −40 to 40 V ($V_{ds} = 0.5$ V) at room temperature. It can be seen that the measured S_{Id}/I_d^2 curves are well matched with $1/f$. The same measurements were also performed at temperatures of 325–400 K. The γ was extracted from the slope of fitting lines under various temperatures and gate biases as shown in Figure 5. It is observed that Device A shows a much smaller variation with temperature, indicating a more stable performance compared with Device S. The γ value indicates the trap location, i.e. $\gamma < 1$ indicates that a trap density is likely near the channel interface and vice versa for $\gamma > 1$ [58, 59]. As the

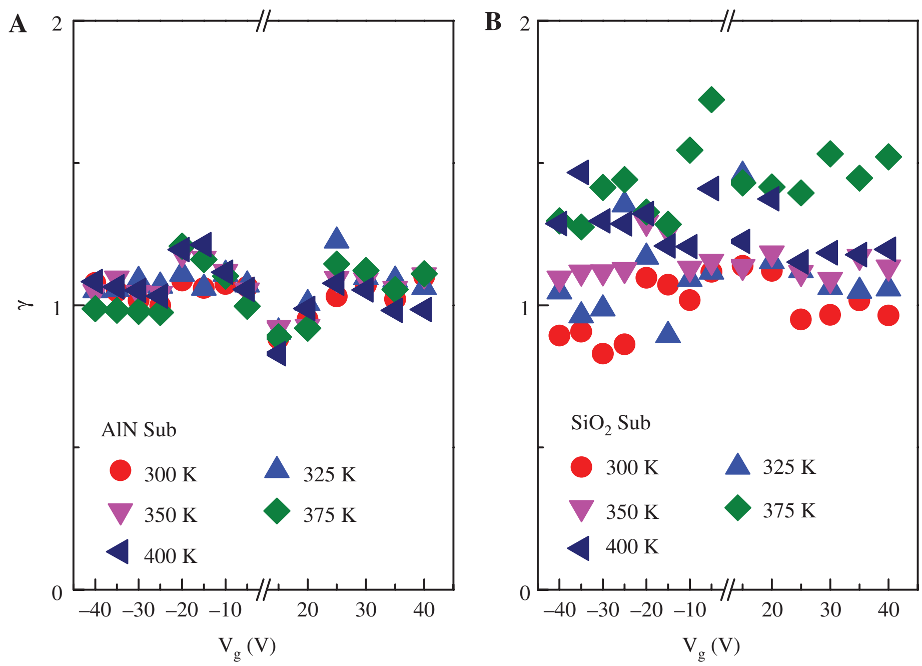

Figure 5: LFN characteristics of BP FETs as functions of frequency and temperature.
The value of γ extracted from the slope of fitting lines of LFN for BP FETs on (A) AlN/SiO_2/Si and (B) SiO_2/Si at different temperatures and gate biases.

temperature rises, the γ of Device S is observed more than once, suggesting that the deep traps in SiO_2 dielectric were activated. However, the γ of Device A remains almost unchanged.

There are two widely accepted mechanisms to explain the $1/f$ noise in the field-effect transistors [60, 61]. One associated with the fluctuations of carrier mobility is known as the Hooge noise model [58, 60], and the other related to the carrier number fluctuations is known as the McWorther model [58, 61]. Our results show that in the p-branch of both types of BP FETs, the LFN in the subthreshold region obeys the carrier number fluctuations model, whereas in the liner region, it follows the fluctuations of the carrier mobility model. In contrast, in the n-branch of the BP FETs on the SiO_2 substrates, the LFN is mainly caused by the fluctuation of carrier mobility, as detailed in Figures S5 and S6. Based on these observations, we separated the region into linear and subthreshold portions for further discussion.

The pFETs noise behaviors in subthreshold (Figure 6A and B) and linear (Figure 6C and D) regions were examined quantitatively. Under various temperatures, the noise levels of Device A were observed more consistent than that of Device S. The noise level of the latter is initially similar to Device A at room temperature, but it increases by several orders of magnitude at high temperature. The carrier mobility fluctuation is mainly caused by lattice or phonon scattering of the carrier, and it is often well fitted in the linear region as follows [60, 61]:

$$\frac{S_{Id}}{I_d^2} = \frac{\alpha_H}{fN} \tag{2}$$

where α_H is the Hooge parameter depending on the crystal quality. A high-quality material often exhibits smaller α_H ranging from 10^{-1} to 10^{-7}. With $N = \frac{Q_i}{q}$ and $Q_i = C_{ox}(V_{gs} - V_T)$, the equation above can be written as follows:

$$\frac{S_{Id}}{I_d^2} = \frac{q\alpha_H}{fWLC_{ox}(V_{gs} - V_T)} \tag{3}$$

Carrier number fluctuation is mainly attributed to the trapping-detrapping process, which is associated with the subthreshold region. The trap density (N_t) can be estimated by the following equation derived from the McWorther model [58, 61]:

$$N_t = \frac{S_{Id} f^{\gamma} WLC_{ox}^2 (V_{gs} - V_T)^2}{I_d^2 q^2 kT\lambda} \tag{4}$$

where λ is the tunneling attenuation length in the gate oxide (≈1 Å). The interface trap density N_{it} can be deduced with $N_t = \lambda N_{it}$.

The Hooge parameter in the linear region and the charge trapped density in the subthreshold region were

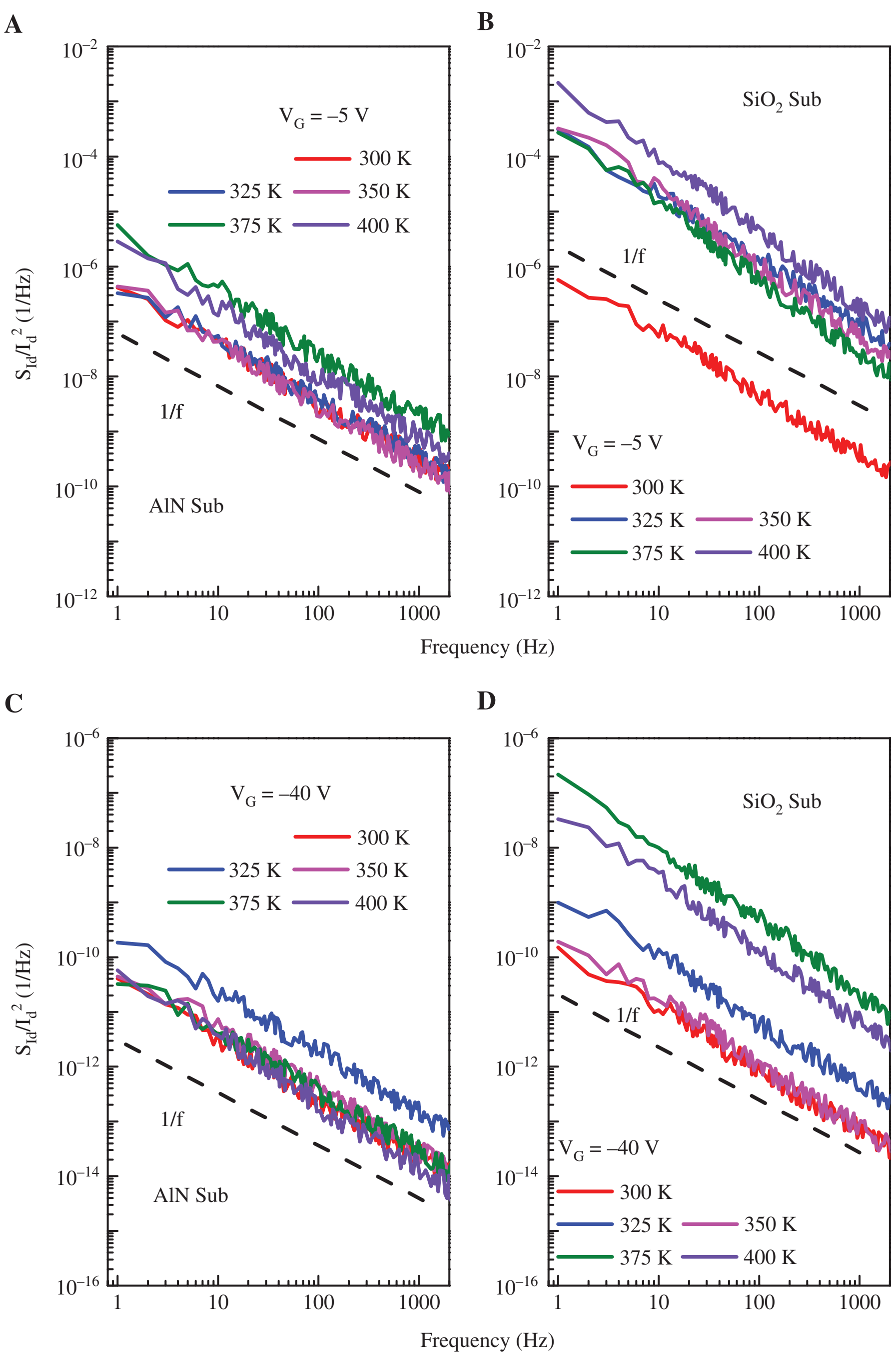

Figure 6: The extracted γ for BP FETs at different temperatures and gate biases.
Low-frequency noise (LFN) characteristics of BP FETs as a function of frequency and temperature on substrate of (A) $AlN/SiO_2/Si$ and (B) SiO_2/Si in the subthreshold region ($V_G = -5$ V), and (C) $AlN/SiO_2/Si$ and (D) bare SiO_2/Si in the linear region ($V_G = -40$ V).

depicted in Figure 7A and B, respectively. The α_H of Device A is observed at around 5×10^{-4} at 300 K and above, whereas α_H of Device S is observed to increase drastically at 350 K. A small α_H indicates a modest lattice scattering even at high temperature. Similarly, the N_{it} in the subthreshold region follows the same characteristic as α_H in Figure 7A, which remains at ~10^{12} with an increased temperature, as shown in Figure 1B. This is within the interface trap density range in semiconductors and insulators [47, 62, 63]. As for BP FTEs on the SiO_2 substrate, the N_{it} increases drastically by 3 orders of magnitudes at 400 K. These observations suggest that the AlN interlayer, with higher surface phonon energy and electrical constant, suppresses the lattice scattering effect and reduces

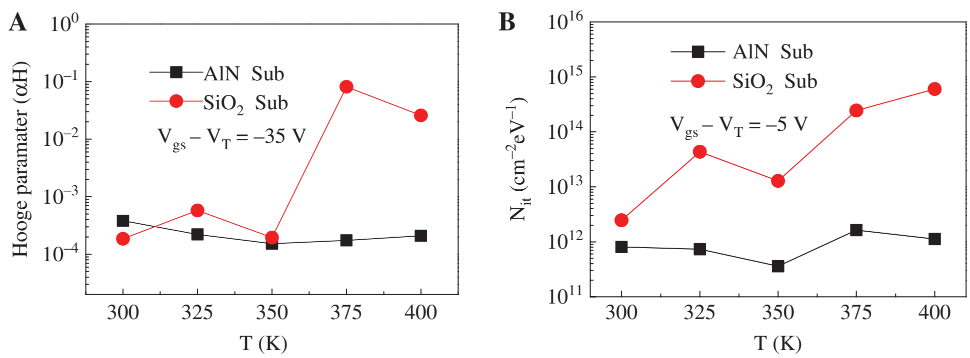

Figure 7: Comparison of calculated α_H and N_{it} for BP FETs on two substrates.
Comparison of (A) Hooge parameter (α_H) in the linear region and (B) interface charge trapped density (N_{it}) in the subthreshold region of BP FETs on different substrates calculated according to the Hooge noise model and the McWorther model, respectively.

the charge trapping impact at high temperature, thus contributing to a stable carrier mobility performance.

4 Conclusion

In summary, it is demonstrated that BP FETs fabricated on the AlN/SiO_2/Si substrate exhibit superior electrical characteristics compared with those fabricated on the conventional SiO_2/Si substrate. The former shows a better on/off current ratio, a lower subthreshold swing, and a higher carrier mobility. Furthermore, it shows that the electrical performance of the BP FETs on the AlN/SiO_2/Si substrate is relatively stable even at high temperatures of up to 400 K, whereas the electrical performance of the BP FETs on the SiO_2/Si substrate degrades drastically. The improved performance is attributed to the presence of the AlN film possessing higher surface phonon energy, therefore effectively suppressing the lattice scattering effect at high temperature. This explanation is further supported by low-frequency noise analysis. It is observed that the BP FETs on the AlN substrate show stable α_H and interface trap density N_{it} from 77 to 400 K, indicating that the lattice scattering and charge trapping at the interface are insensitive to the high temperature. As a result, the BP FETs on the AlN substrate with a more stable carrier mobility performance compared with that on the SiO_2 substrate are achieved in this work.

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