Abstract: This paper proposes a generalized carrier-based pulse-width modulation (CBPWM) method for a 12-switch converter feeding three independent loads. The converter topology is part of the \((3N+3)\)-switch converter family where \(N\) is the number of outputs \((N = 3\) for this special case). Its more famous sibling is the 9-switch converter which is gaining considerable interest from researchers because of its reduced-switch count architecture. The structure and limitations of the converter are elaborated; its modulation method applicable to both equal and different frequency (and/or amplitude) operations is formulated. The generalized neutral voltages for the converter is derived for the first time and used as the offset voltages required by this type of topology to decouple its three outputs. The proposed algorithm is validated by both theoretical simulations and experimental results.

Keywords: reduced-switch-count; nine-switch inverter; carrier-based pwm; ac drive; twelve-switch inverter

1 Introduction

In most modern industrial processes, high-performance control of AC machines is achieved using voltage source converters (VSCs). A typical process may require independent control of several AC machines. Usually, this function is implemented using a separate converter per machine. However, in medium to high power applications, the cost of power electronics becomes an important design constraint. An increasingly accepted alternative to full-switch count VSCs is to use reduced-switch count VSC topologies [1–14]. The 5–leg inverter [1, 2]; 4-leg inverter [3, 4]; 6- and 3-switch converters [5]; 4-switch inverter [6]; 9-switch inverter [10–14]; and multilevel converters [8, 9] are but a few examples.

Most of the reduced-switch count topologies can be categorized into three main types; in the first category, reduction in switch count is achieved by replacing a switched-leg with a split-capacitor-leg and sharing this split-capacitor-leg between two outputs (or phases) [5, 6]. The drawback of this topology is the appearance of unbalance capacitor voltages and the associated uneven stress on the devices. An improved topology replaces the capacitor-leg with a switched-leg. These are the so-called \((2n + 1)\)-leg converters [7] and the 5–leg converter is special case of this type [1, 2]. A third type of reduced-switch count VSCs which has gained prominence lately, is implemented by sharing a row of switches between neighboring outputs (or phases). The 9-switch converter [10–14] is an example of this type. In fact, the 9-switch converter can be considered as a special case of the generalized \((3N+3)\)-switch converter introduced in [10] for \(N = 2\) \((N\) represents the number of independent three-phase outputs). The 6-switch converter [5] is a hybrid of the split-capacitor-leg[5, 6] and the \((3N+3)\)-switch topologies [10–15].

The net gain from using reduced number of switching devices in VSCs may at first seem insignificant. For example, in the 5–leg topology [1, 2] there is a reduction of only two switching devices compared to the full-switch topology. However, the reduced-switch count is accompanied by elimination of accompanying complex gate driver and protection circuits. Thus, the overall system can be significantly less expensive, smaller size and lighter in weight. These gains, however, come with structural limitations. The sharing of legs or switches between outputs (or phases) inherently couples the sharing partners and imposes switching constraints on the converter that must be catered for by an appropriate switching algorithm.

Since the 9-switch was first introduced [10–12], several researches have attempted to remedy its shortcoming and thereby increase its appeal. These efforts have resulted in applications such as uninterruptible power supplies (UPS) [12, 16], adjustable speed motor drive [13], six-phase motor drive [17], unified power quality conditioner...
2 Structure and Switching Limitations

Fig. 1 shows the structure of the \((3N + 3)\)-switch converter supplying \(N\) independent three-phase induction machines (IMs). The switching devices are represented by \(Q_{ij}\) where the subscript \(i \in \{a, b, c\}\) refer to the three phases and the second index, \(j \in \{1, 2, \ldots, N + 1\}\), show the position of a switch in a phase-leg. The machines (or outputs) are represented by \(\text{IM}_k\) (or \(\text{Inv}_k\)) where \(k \in \{1, 2, \ldots, N\}\) refer to the position of the machine (or output) in the \(N\)-machine (or \(N\)-output) system.

In this paper, it is assumed that the neutral points, \(z_k\), of the machines are isolated from one another. A distinct feature of this topology is the sharing of row of switches between neighboring outputs. Except for the topmost and bottommost switch rows (i.e. \(k = 1\) and \(k = N\)), which have a single neighboring switch each, all the inner switches have two neighbors each. The classical 6-switch, 9-switch \([10–14]\), and the 12-switch converters \([10]\) are special cases of the generalized \((3N + 3)\)-switch converter for \(N = 1, 2, 3\), respectively. Like with most reduced-switch count topologies, the switch operations are constrained by the sharing of switches between outputs. For the \((3N + 3)\)-switch configuration, there are \(2^{(3N+3)}\) possible conduction states of all switches and can be represented by switching functions \(S_{ij} \in \{0, 1\}\). \(S_{ij} = 1\) if switch is conducting and \(S_{ij} = 0\) if not conducting.

To ensure Kirchoff’s current and voltages laws are obeyed and that there is current continuity, the relationship between the switching functions per phase-leg can be shown to be given by

\[
\sum_{j=1}^{N+1} S_{ij} = N; \quad i \in \{a, b, c\}; \quad j \in \{1, 2, 3, \ldots, N + 1\}. \quad (1)
\]

The pole voltages for \((3N + 3)\)-switch topology can be derived from Fig. 1 and are, respectively given as

\[
V_{iko} = V_{ikz} + V_{zko} = 0.5V_{dc} \left( \prod_{j=1}^{k} S_{ij} - \prod_{j=k+1}^{N+1} S_{ij} \right);
\]

\[
k \in \{1, 2, 3, \ldots, N\} \quad (2)
\]

with \(V_{zko}\) being the neutral (otherwise known as common-mode) voltages; \(V_{ikz}\) refer to the phase-to-neutral voltages; \(z\) is the neutral point of the IM stator windings; \(V_{dc}\) is the input DC voltage and \(o\) is its virtual midpoint. Fig. 1 shows the outputs share row(s) of switches with their neighbors and are therefore coupled. If independent control of the \(N\) IMs (variable frequency and/or amplitude) is desired, then...
a modulation strategy to decouple the outputs should be developed. The proposed PWM strategy is discussed in the proceeding section.

3 Proposed PWM method

The Pulse-Width Modulation (PWM) method developed in [15] for the two, three-phase loads using the 9-switch topology, can be extended to an arbitrary N-machine drive. Since the conventional Space Vector Pulse-Width Modulation (SVPWM) and carrier-based PWM schemes are equivalent and lead to the same output voltages, only the latter is discussed in detail in this paper. However, the authors make use of the former only to derive the neutral voltages, \( V_{zko} \), which is injected into reference commands to extend the modulation index range in the linear modulation region. More importantly, the injection of \( V_{zko} \) decouples the \( N \) outputs. The basic idea of the proposed modulation is to use only switching states that decouple the \( N \) outputs and then utilize standard PWM modulators.

3.1 Introduction to Space Vector for 12-switch Converter

The SVPWM technique construct the desired sinusoidal three-phase voltages by selecting feasible switching states of the VSC and calculating their corresponding on-time durations. As \( N \) increases, the number of conducting states of an \((3N + 3)\)-switch converter rises exponentially (i.e. \( 2^{3N+3} \)). However, by virtue of (1), it can be shown that the feasible conducting states reduce significantly to \((N + 1)^3 \). Thus for \( 6 \), \( 9 \), \( 12 \), \( 15 \), and \( 18 \)-switch (i.e. \( N = 1, 2, 3, 4, \) and \( 5 \)) topologies; the feasible conducting states are, respectively, \( 8, 27, 64, 125, \) and \( 216 \). The pole voltages given by (2) can be used to map each of the \((N + 1)^3 \) states into a voltage space-vector in the complex plane using Clarke’s transformation [26].

For the 12-switch converter, there are sixty-four (64) feasible switching states obtained using (1). The \( abc \) pole voltages can be calculated from (2) and the corresponding \( qd0 \) voltages are calculated using Clarke’s Transformation[26]. The space vector plot for all 64 states are shown in Fig. 2. The following inferences can be made from Fig. 2:

- There are twenty-eight (28) zero sequences voltages for \( \text{Inv} 1 \) and \( \text{Inv} 3 \); sixteen (16) for \( \text{Inv} 2 \). However, only four (i.e. 1, 22, 43, and 64) are common to all three outputs. These are the decoupling zero states for this topology.
- There are at least three active states at each vertex of the hexagon.
- The active states \{33, 41, 9, 11, 3, and 34\}, form the vertices of the space vector hexagon and produce equal vectors for all three outputs. If equal frequency operation is desired, then these states may be used.
- The active states \{17, 21, 5, 6, 2, and 18\}; \{54, 62, 30, 32, 24 and 56\}; and \{48, 44, 60, 59, 63 and 47\}, respectively form the vertices of the space vector hexagons of the three outputs. Since these active states produce zero states in the other two outputs, they can be used to effectively decouple the three outputs. These states are the only active states (in addition to the 4 decoupling zero states) allowed in the proposed PWM scheme and are tabulated in Table 1.

3.2 Switching Sequences

After decoupling the three outputs, each three-phase output can be viewed as an ‘independent’ VSC with its own space vector hexagon as shown in Fig. 3. There are many choices for the arrangement of the switching vectors to achieve the desired output voltages, but only the conventional switching sequence [26, 27], is adopted in this paper for simplicity, and without loss of generality. In the conventional SVPWM, two active vectors are applied between the two zero vectors for the case of the 6-switch converter (e.g. \( 0 - 1 - 2 - 7 \) or \( 7 - 2 - 1 - 0 \) [26, 27]). In this work, the zero states are represented by the code numbers 0, and the active states vectors by \( 1^k \) and \( 2^k \) where the bracketed superscript, \( k \), represents the \( k \)th output. For example, the switching sequences for the 9-, and 12-switch converters are, respectively:

9-switch \((N = 2)\) : 01 - 1(1) - 2(1) - 03 - 1(2) - 2(2) - 02
12-switch \((N = 3)\) : 01 - 1(1) - 2(1) - 02 - 1(2) - 2(2) - 04 - 1(3) - 2(3) - 03.

3.3 Generalized Neutral Voltages

The CBPWM scheme of the \((3N + 3)\)-switch converter is based on injecting DC voltages [10–14, 25] or neutral voltage(s) [15] into the reference modulating signals in order to decouple all \( N \) outputs. Using the decoupled space hexagons (see Fig. 3) and the switching sequence adopted above, the neutral voltages for the 12-switch converter can be found in terms of the active and zero vectors dwell
times. In the proposed PWM method, for generality, it is assumed that all \(4(N + 1 = 4)\) zero states are used in synthesizing the reference voltages. The dwell time for the zero states is shared among all 4 states according to distribution factors \(a_j \in [1, 2, 3, 4]\). Note that \(\sum_j a_j = 1\) and \(0 \leq a_j \leq 1\).
Table 1: Switching states for independent control of Inv1, Inv2, and Inv3.

<table>
<thead>
<tr>
<th>Switching states</th>
<th>Transformed pole voltages</th>
</tr>
</thead>
<tbody>
<tr>
<td>Label</td>
<td>$V_{q1}$</td>
</tr>
<tr>
<td>$V_{1}^{(1)}$</td>
<td>17</td>
</tr>
<tr>
<td>$V_{2}^{(1)}$</td>
<td>21</td>
</tr>
<tr>
<td>$V_{3}^{(1)}$</td>
<td>5</td>
</tr>
<tr>
<td>$V_{4}^{(1)}$</td>
<td>6</td>
</tr>
<tr>
<td>$V_{5}^{(1)}$</td>
<td>2</td>
</tr>
<tr>
<td>$V_{6}^{(1)}$</td>
<td>18</td>
</tr>
<tr>
<td>$V_{1}^{(2)}$</td>
<td>54</td>
</tr>
<tr>
<td>$V_{2}^{(2)}$</td>
<td>62</td>
</tr>
<tr>
<td>$V_{3}^{(2)}$</td>
<td>30</td>
</tr>
<tr>
<td>$V_{4}^{(2)}$</td>
<td>32</td>
</tr>
<tr>
<td>$V_{5}^{(2)}$</td>
<td>24</td>
</tr>
<tr>
<td>$V_{6}^{(2)}$</td>
<td>56</td>
</tr>
<tr>
<td>$V_{1}^{(3)}$</td>
<td>48</td>
</tr>
<tr>
<td>$V_{2}^{(3)}$</td>
<td>44</td>
</tr>
<tr>
<td>$V_{3}^{(3)}$</td>
<td>60</td>
</tr>
<tr>
<td>$V_{4}^{(3)}$</td>
<td>59</td>
</tr>
<tr>
<td>$V_{5}^{(3)}$</td>
<td>63</td>
</tr>
<tr>
<td>$V_{6}^{(3)}$</td>
<td>47</td>
</tr>
<tr>
<td>$V_{01}$</td>
<td>1</td>
</tr>
<tr>
<td>$V_{02}$</td>
<td>22</td>
</tr>
<tr>
<td>$V_{03}$</td>
<td>43</td>
</tr>
<tr>
<td>$V_{04}$</td>
<td>64</td>
</tr>
</tbody>
</table>

*Note: $V_{ab}$ and $V_{ok}$ are multiples of $\sqrt{2/3} \times V_d$ and that of $V_{dk}$ are multiples of $\sqrt{2/3} \times V_f$.

$\alpha_j \leq 1$. For example, if the reference voltages are located in arbitrary sectors, $(x^{(1)}, x^{(2)}, x^{(3)}); x \in \{I, II, III, IV, V, VI\}$, the corresponding average neutral voltages over a switching period $T_s$ can be approximated as:

$$
\langle V_{zko} \rangle = \frac{1}{3} \sum_{k=1}^{3} (V_{a1}^{(k)}t_{a1}^{(k)} + V_{b1}^{(k)}t_{b1}^{(k)}) + \sum_{j=1}^{4} V_{oj}t_{oj}
$$

$$
k = 1, 2, 3; \ j = 1, 2, 3, 4
$$

where $V_{a1}^{(k)}$ and $V_{b1}^{(k)}$ are the respective zero sequence voltages of the two nearest adjacent active vectors; $V_{oj}$ represent the zero vectors; and $t_{a1}^{(k)}, t_{b1}^{(k)}$, and $t_{oj}$ are their corresponding dwell times. For simplicity and without loss of generality, assume that at some point in time, the 3 reference voltages are located in sectors $(I^{(1)}, II^{(2)}, I^{(3)})$ as shown in Fig. 3. The neutral voltages for the 12-switch topology, from (3) and Table 1 can be expressed as in (4)

$$
V_{z1o} = \Gamma \left[ 3 (-t_{01} + t_{02} + t_{03} + t_{04}) + \xi (t_{a1}^{(1)} + t_{b1}^{(1)}) + 3 (t_{a1}^{(2)} + t_{b1}^{(2)}) + 3 (t_{a1}^{(3)} + t_{b1}^{(3)}) \right]
$$

$$
(4a)
$$

$$
V_{z2o} = \Gamma \left[ 3 (-t_{01} + t_{02} - t_{03} - t_{04}) + \xi (-t_{a1}^{(1)} + t_{b1}^{(1)}) + 3 (t_{a1}^{(2)} + t_{b1}^{(2)}) + 3 (t_{a1}^{(3)} + t_{b1}^{(3)}) \right]
$$

$$
(4b)
$$

$$
V_{z3o} = \Gamma \left[ 3 (-t_{01} - t_{02} + t_{03} - t_{04}) + \xi (t_{a1}^{(1)} + t_{b1}^{(1)}) + 3 (t_{a1}^{(2)} + t_{b1}^{(2)}) + 3 (t_{a1}^{(3)} + t_{b1}^{(3)}) \right]
$$

$$
(4c)
$$

where $\xi = +1$ for odd sectors, $\xi = -1$ for even sectors, and $\Gamma = \sqrt{2/3} \times \frac{V_f}{V_d}$. The neutral voltage expressions in (4) can be generalized for any sector combination by expressing the dwell times in terms of the maximum and minimum phase voltages in each combination [15], resulting in (5). In (5): $q \in \{2, 3, 4, \ldots, N - 1\}$ is the machine (output) position except the topmost or bottommost machines (outputs); $v_{max,k} = \max(V_{akz}, V_{bkz}, V_{ckz})$ and $v_{min,k} = \min(V_{akz}, V_{bkz}, V_{ckz})$

$$
V_{z1o} = 0.5V_{dc} (1 - 2a_1) - v_{max,1} + a_1 \sum_{k=1}^{3} (v_{max,k} - v_{min,k})
$$

$$
(5a)
$$
3.4 Modulation Method

In the classical two-level three-phase converter, the neutral voltages offer degrees of freedom that may be used to improve the DC bus utilization and lower output current ripple without appearing in either the line-to-line or phase voltages of the three-phase machines [7]. In the $(3N + 3)$-switch topology, the neutral voltage(s) can be used to decouple all $N$ outputs by modifying the reference modulation signals such that $k^{th}$ modulation signal is always greater than the $(k+1)^{th}$ modulation signal [10–14]. In general, modulation signals for the carrier-based modulator are given by [7]:

$$M_{ikz} = \frac{2}{V_{dc}} \left( V_{ikz} + V_{zko} \right) = \frac{2}{V_{dc}} \left( m_{ikz}^* + m_{zko} \right)$$

$$i \in \{a, b, c\}; \quad k \in [1, 2, \ldots, N]$$

(6)

where $m_{zko}$ represent the normalized neutral voltages (w.r.t. $0.5V_{dc}$), and $m_{ikz}^*$ are the normalized fundamental sinusoidal reference signals (also w.r.t. $0.5V_{dc}$).

The structure of the proposed carrier-based three-phase modulator, including the neutral voltage injection, is shown in Fig. 4. The modulating signals are compared with a high-frequency carrier signal, and, as a result, gate signals are generated for each phase. In the 12-switch topology, there are 3 modulating signals per phase-leg and one high frequency carrier signal, $v_{tri}$. To satisfy the switching function constraints (1), they are generated using the logic given in (7) and illustrated by Fig. 4. The injection of the neutral voltages allows the three modulation signals to be separated such that at any instant, the $M_{ikz}$ is always greater than $M_{(ik+1)z}$, which is a requirement for this converter topology to satisfy the switching function constraint specified by (1).

$$S_{i1} = \begin{cases} 1, & \text{if } M_{i1z} \geq v_{tri} \\ 0, & \text{if } M_{i1z} < v_{tri} \end{cases}$$

$$S'_{i2} = \begin{cases} 1, & \text{if } M_{i2z} \geq v_{tri} \text{ or } M_{i1z} \geq v_{tri} \\ 0, & \text{if } M_{i2z} < v_{tri} \end{cases}$$

(7a)

$$S_{i2} = S_{i1} + S'_{i2}$$

(7b)

Figure 3: Decoupled space vector hexagons of 12-switch converter for (a) Inv1, (b) Inv2, and (c) Inv3.
\[ S_{i3}' = \begin{cases} 1, & \text{if } M_{i32} \geq V_{tri} \\ 0, & \text{if } M_{i32} < V_{tri} \end{cases}; S_{i3} = \overline{S_{i3}'} + S_{i3}' \quad (7c) \]

where \( \overline{S_{ij}} \) is the logical NOT operator and \( S_{ij}' \) is as defined in Fig. 4a.

4 Simulation and experimental results

Matlab/Simulink simulations and experiments were performed to validate the proposed PWM scheme. Table 2 gives the converter parameters used for both simulations and experimental setup.

4.1 Simulation Results

In general, for the \((3N+3)\)-switch topology, there are \(N+1\) zero vectors with dwell time distribution factors, \(a_j\), whose values give rise to infinite PWM schemes. Fig. 5 illustrates the modulation signals for continuous and discontinuous CBPWM. In the continuous CBPWM, the dwell time for the zero vectors is evenly shared among the 4 zero vectors (i.e. \(a_1 = a_2 = a_3 = a_4 = \frac{1}{4}\)), which correspond to the classical SVPWM for the two-level VSC when \(a_1 = a_2 = 0.5\). This is shown in Fig. 5a. Infinite discontinuous PWM are possible just by defining the zero dwell times. For example, Fig. 5b, shows the zero vectors distribution defined by

\[ a_j = \frac{1}{6} (1 + \text{sgn}(3\omega_k t + \delta_k)) \quad k \in [1, 2, 3] \]

\[ j \in [1, 2, 3, 4] \quad (8) \]

where \( \text{sgn}(X) = 1, 0 \) or \(-1\) for \(X > 0, X = 0\) and \(X < 0\), respectively; \( \omega_k \), is the fundamental frequency of the \(k\)th reference voltage. and \( \delta_k \) is the corresponding modulation angle. Observe that in Fig. 5b, even though the topmost and bottommost switches are clamped to the positive and negative DC rails, respectively for 60 deg of the switching period, the inner switches do not experience any DC clamping. Due to space limitations, the simulated current and voltage waveforms are shown for only the continuous CBPWM.

In Fig. 5a, the reference (left) and derived (right) modulation signals are shown for the continuous CBPWM case. It can be observed that the injection of the neutral voltage ensure that at any instant, \(M_{ikz}\) is always greater than \(M_{i(k+1)z}\). The corresponding phase \(a\) voltages, and phase \(abc\) load currents (and their harmonic spectra) are shown in Figs. 6a, 6b, and 6c, respectively. In Fig. 6a, the generated voltages are shown with the low frequency components and reference voltages overlaid on each other; the results validate the proposed algorithm. Fig. 6b show that the phase currents are less noisy with the spectra showing peaks at 95, 60, and 25 Hz, respectively. Finally, Fig. 6c show the input DC current and the corresponding harmonic spectrum. The spectrum of the DC current show three low frequency peaks at 0, 35, and 70 Hz. Since the input DC current is summation of the phase currents, the peaks at 30 and 70 Hz come about as a result of the different frequency operation.

![Figure 4: 12-switch converter CBPWM modulator: (a) block diagram of switching logic, and (b) triangle intersection of N modulation signals.](image-url)

Table 2: Parameters of simulations and experimental setup.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase a1 (V_1/V, f_1/Hz)</td>
<td>(0.5V_{dc}/\sqrt{3}; 95)</td>
</tr>
<tr>
<td>Phase a2 (V_2/V, f_2/Hz)</td>
<td>(0.3V_{dc}/\sqrt{3}; 60)</td>
</tr>
<tr>
<td>Phase a3 (V_3/V, f_3/Hz)</td>
<td>(0.2V_{dc}/\sqrt{3}; 25)</td>
</tr>
<tr>
<td>Switching frequency/kHz</td>
<td>1.0</td>
</tr>
<tr>
<td>(V_{dc}/V)</td>
<td>50.0</td>
</tr>
<tr>
<td>(R/\Omega; L/mH)</td>
<td>0.3; 1.05</td>
</tr>
</tbody>
</table>
Figure 5: 12-switch simulated phase α modulation signals: reference (left) and derived (right) for (a) continuous and (b) discontinuous CBPWM.
4.2 Experimental Results

A laboratory prototype of the 12-switch (can be configured for 9-switch) converter was designed and built; its photograph is shown in Fig. 7. The gate PWM signals were generated using a dSPACE ds1104 real-time controller. The 12-switch converter supplies three independent three-phase \textit{RL} loads with the same nominal parameters as those used in the simulations. The switching frequency of the inverter is set to 1 kHz and the input DC is 50 V DC. The inverter dead time is approximately 8 µs. Illustrative waveforms of line voltage and phase voltages, phase and input DC currents are shown in Figs. 8a–8c. Even though the aforementioned experimental waveforms show some spikes especially that of \textit{Inv} 3 (25 Hz) in Fig. 8c, by and large, the waveforms show strong correspondence between simulations and experiments comparing the respective figures. The experiments thus validate the proposed method.

5 Conclusions

The CBPWM method for the 12-switch converter has been proposed. To the best of the authors knowledge, the generalized neutral voltages for the converter have been derived for the first time in this paper and used as the offset voltages required by this topology to decouple the converter’s three outputs. Additionally, the neutral voltages can be used to modify the modulation schemes for various drive applications just by specifying the null voltages dwell time distribution. The proposed algorithm has been validated by both theoretical simulation and experimental results. The results show that the desired voltages have been correctly synthesized.

Figure 6: 12-switch simulated waveforms for \textit{Inv} 1, \textit{Inv} 2 and \textit{Inv} 3: (a) phase \textit{a} voltages (\textit{Inv} 1: top, \textit{Inv} 2: middle, and \textit{Inv} 3: bottom), (b) phase currents (\textit{Inv} 1: top, \textit{Inv} 2: middle, and \textit{Inv} 3: bottom), and (c) input DC current and its harmonic spectrum.

Figure 7: photo of 12-switch converter prototype
Note: All currents have been scaled down by a factor of 100.

Figure 8: Experimental waveforms: line voltage (Ch1), phase voltage (Ch2), phase current (Ch3), and input DC current (Ch4) for (a) Inv1; 95 Hz, (b) Inv2; 60 Hz, and (c) Inv3; 25 Hz respectively.

References


