Review article

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Silicon photonic devices and integrated circuits

Abstract: Silicon photonic devices and integrated circuits have undergone rapid and significant progresses during the last decade, transitioning from research topics in universities to product development in corporations. Silicon photonics is anticipated to be a disruptive optical technology for data communications, with applications such as intra-chip interconnects, short-reach communications in datacenters and supercomputers, and long-haul optical transmissions. Bell Labs, as the research organization of Alcatel-Lucent, a network system vendor, has an optimal position to identify the full potential of silicon photonics both in the applications and in its technical merits. Additionally it has demonstrated novel and improved high-performance optical devices, and implemented multi-function photonic integrated circuits to fulfill various communication applications. In this paper, we review our silicon photonic programs and main achievements during recent years. For devices, we review high-performance single-drive push-pull silicon Mach-Zehnder modulators, hybrid silicon/III-V lasers and silicon nitride-assisted polarization rotators. For photonic circuits, we review silicon/silicon nitride integration platforms to implement wavelength-division multiplexing receivers and transmitters. In addition, we show silicon photonic circuits are well suited for dual-polarization optical coherent transmitters and receivers, geared for advanced modulation formats. We also discuss various applications in the field of communication which may benefit from implementation in silicon photonics.

Keywords: optical communication; optical interconnect; photonic integrated circuits; silicon photonics.

1 Introduction

There exist a variety of definitions as to what does or does not constitute silicon photonics. Avoiding semantic arguments we shall simply give our practical definition of silicon photonics, which is based on the goal of achieving very large-scale integration (VLSI) of photonics. Therefore, we consider silicon photonics to be optical devices and circuits, which satisfy two conditions. The first is that silicon-core waveguides must be used in at least part of the devices or circuits to provide compact optical devices, which allow high-density integration. Secondly, fabrication of the devices should use whole-wafer processing or equivalent techniques that would be allowed in a complementary metal-oxide-semiconductor (CMOS) fabrication facility to allow large-scale low-cost manufacturability.

To illustrate we will consider some examples. Under this definition, a planar lightwave circuit (PLC) based on silica waveguides is not a silicon photonic device although it may be fabricated on a silicon substrate in a CMOS fab. Germanium photo detectors on silicon can be silicon photonic devices as germanium can be directly grown on silicon and be processed in a wafer scale afterwards [1]. A hybrid laser fabricated by wafer bonding between III and V wafers and silicon-on-insulator (SOI) wafers [2] may be a silicon photonic device only if the bonding technique used allows the full-wafer processing in the following fabrication steps.

The motivation for the first requirement can be illustrated by the many benefits coming from using silicon as a waveguide core. With silicon oxide as the cladding, silicon waveguides have an index contrast of ~2 and allow sub-micrometer cross-sectional dimensions. Typically, waveguide widths of ~0.5 µm and waveguide heights of 0.2–0.3 µm are employed for submicron silicon photonics. The greater width over height results in lower waveguide propagation loss since the loss mainly results from the scattering at etched sidewalls. With this waveguide geometry, a tight bending radius <5 µm is permitted. The tight bends result in extremely compact optical components and hence flexible circuit design, which are crucial for very large-scale photonic integration. Due to the high index contrast, silicon waveguides can also expand the
mode sizes to a few microns to match the mode of optical fibers by shrinking the core size, usually called inverse tapers [3–5]. Compact grating structures which can efficiently couple the light between silicon waveguide guiding modes to out-of-plane fiber modes, are also enabled by the high index contrast [6–9]. In addition, because of the large difference between waveguide width and height, submicron silicon waveguides could have a large index difference between the transverse-electrical (TE) and transverse-magnetic (TM) modes. This large birefringence can be used to make very compact and efficient polarization splitters and polarization rotators [10–14], which are ideal for constructing polarization-diversified photonic integrated circuits (PICs).

Wafer-scale CMOS fabrication enables silicon photonics to be a viable platform for very large-scale photonic circuits with high yield and low cost, by exploiting existing and mature fabrication facilities and processes. The CMOS industry has developed large-size silicon wafers with low defect densities, which is particularly critical to achieve large-scale photonics circuits. Silicon CMOS allows many types of materials such as silicon oxide, silicon nitride, germanium, and various metals. This enables feasible process integration of various active and passive photonic devices such as splitters, couplers, modulators, photo detectors, and thermal phase shifters. By allowing the integration of more optical functions on single chips, the packaging cost can be greatly reduced.

Finally, if we are to achieve the goal of monolithic electronic and photonics integrated circuits on silicon [15], then the photonic device fabrication must use a compatible process. Monolithic integration of silicon PICs with CMOS drivers leads to more complex optical functions being practical, and with lower power consumption and lower packaging cost. Furthermore, on-chip optical interconnects offered by integration of silicon photonics with electronic integrated circuits (ICs) are expected to solve the interconnect bottlenecks of modern electronic ICs.

Bell Labs, Alcatel-Lucent, has been actively involving in the development of silicon photonics devices and circuits for many years. In this paper, we review some of Bell Labs major achievements in this area. The organization of this paper is as follows. In the next section, we review applications and motivations of silicon photonics in different communication areas. In Sections 3 and 4, we review Bell Labs developed silicon photonics devices and circuits including high-bandwidth silicon modulators, hybrid lasers, polarization rotators/combiners/splitters, wavelength-division multiplexing (WDM) transmitters, WDM receivers, dual-polarization coherent transmitters and receivers. We emphasize that this paper focuses on silicon photonic devices and circuits from Bell Labs, rather than a comprehensive review of all work in silicon photonics.

2 Applications

Much of the work on silicon photonics has been targeted primarily at applications in chip-level (including intra-chip and inter-chip) optical interconnects, where it is expected to solve the bottlenecks of metal electrical interconnects at high data rates. Our work focuses primarily on the applications in telecommunications and short-reach interconnects where optical systems are already being used, but where there is a need for increased integration. In this section, we discuss the applications and motivations using silicon photonics in long-haul and metro coherent transmissions, as interconnects for routers and switches, and as short-reach communications in datacenters and supercomputers.

2.1 Long-haul/metro coherent optical networks

In the past decades, the capacity of the core optic network has been growing significantly, driven by the ubiquitous multi-media users, vast data centers and cloud-based applications. To meet this demand, the 100 Gb/s channel data rate transponders are currently being deployed in the long-haul optic fiber transport network and the per channel rates will continue to grow to 400 Gb/s and 1 Tb/s while expanding into metro and datacenter fiber networks within the next decade [16, 17]. Advanced optical modulation formats, such as quadrature phase-shift keying (QPSK), quadrature amplitude modulation (QAM), and orthogonal frequency-division multiplexing (OFDM), in combination with the coherent detection techniques are used to increase the spectral efficiency [18, 19]. These coherent techniques require the use of digital signal processing (DSP) functionality at both the transmitter and receiver to mitigate transmission impairments and maximize channel capacity. These DSP functions are realized on application specific ICs (ASICs) implemented in advanced CMOS. In this way, more data bits can be packed and coded into each optical channel to allow more capacity per fiber. In particular, polarization-division-multiplexed QPSK (PDM-QPSK) is utilized in the current networks for 100-Gb/s transponders. Next-generation networks may utilize even higher modulation formats, such as 16-ary QAM (16-QAM).
Currently, the optoelectronic interfaces in the core network are implemented with discrete component technologies such as InP lasers and detectors, LiNbO$_3$ modulators and silica-based PLCs assembled together with bulk optic elements to deliver the required performance. As the capacity and data rate are increased at high capacity network nodes, it will require smaller footprint, higher optical port density, and lower power consumption. Increased photonic integration will be required and is expected to achieve this goal.

Silicon photonics technology has demonstrated promising results to meet these capacity demands with its capability for high integration level, low energy consumption and, in the near future, with embedded electronic intelligence, with integrated CMOS electronics, to accommodate and mitigate the dynamic network environment. Examples of devices for these applications include dual-polarization QPSK coherent receiver and transmitter silicon PICs demonstrated at 112 Gb/s [20–22]. With its high integration level on a single chip, chip-scale WDM modulator and receiver silicon PICs have been demonstrated [23, 24]. A 1.6 Tb/s receiving capability was implemented in a 40-channel WDM receive PIC with 40 Gb/s data rate per channel [23] as well as a 250 Gb/s 10-channel silicon modulator chip with a 25 Gb/s data rate for each channel [24]. The emerging electronic-photonics co-integration [25, 26] would allow the photonic integrated devices to be combined with the DSP functionality to facilitate capacity scaling and further introduce electronic intelligence to the network node. This would provide optimal adaptation to the dynamic network environment and mitigate many transmission impairments to further enhance the stability and robustness of the core networks and enable new architecture and applications for cloud-based networks.

2.2 Optical interconnects for routers and switches

Packet routing and switching are an essential part of today’s network, enabling services and efficient sharing of network transport resources. While router vendors have provided increasingly large capacity routers they have not been able to achieve reductions in power to match the growth in capacity. Figure 1 shows the scaling over time of the energy per bit routed, for high capacity Internet protocol (IP) routers. The energy per bit routed or switched is falling at around 13.5% per year, less than trend observed previously in 2006 [27]. This rate of reduction matches the feature size reduction of silicon. This is the power scaling that would be expected when an ASIC is limited by its I/O power consumption [28].

Since energy efficiency is not scaling as rapidly as capacity growth this leads to increasing power density (20%/year). High power density leads to increased chip operating temperatures, makes design more challenging and limits the addition of features to routers. Ultimately the largest capacity routers cannot be accommodated within a single rack. Current router systems [29] for multi terabit per second routing include multi rack solutions using optical interconnects between racks. Electrical interconnects have frequency and distance dependent loss which leads to a practical distance bandwidth product limit of around 100 Gb/s.m [30]. Beyond this distance bandwidth product, optical interconnects are typically used with multimode fiber giving way to single mode fiber at around 1 Tb/s.m. This is illustrated in Figure 2 updated from Ref. [30]. Routers and switches have both client side and internal interconnect requirements. The client side interfaces, which will soon be 1 Tb/s per card usually, conform to standards based interfaces, and require reaches of typically 100 m to 80 km. Even implementing 100 m reach 1 Tb/s interface using multimode fiber could require a 100 fiber pairs. Connecting large numbers of fibers results in challenges to footprint both on the linecard boards and faceplate density. Additionally there is a significantly higher cost in providing multi-fiber ribbons. Therefore there is a need for single mode fiber (SMF) interfaces based on the kind of photonic integration that silicon photonics offers, even in the shorter reach space. Additionally there is a need to make long haul interfaces such as those...
described in the previous section available on router line cards, to enable direct connection of routers to long haul transport.

The internal interconnect requirements for routers and switches are typically around twice the bandwidth of the client interface, to account for redundancy and over speed to avoid blocking, though the distances typically are less. For rack to rack interconnect if we assume a minimum distance of 50 m, to allow for placement and cabling, this makes multimode fiber attractive at 2–20 Gb/s range and single mode attractive above 20 Gb/s. With todays routers having backplane interconnect requirements in the range of 10–20 Tb/s this would require around a 1000 multimode fiber pairs. It is clear that if we wish to grow these systems we need to increase the data rate per fiber, which will require the use of SMF and the various techniques such as WDM more commonly associated with longer reach optical communication. Making these practical will require increasing levels of photonic integration and so silicon photonics is an attractive option.

2.3 Datacenters and supercomputers

Datacenters concentrate huge computational resources, including computers, servers, storage, media and networking functions. Datacenter capacity grows both with the increasing volume of Internet traffic and with the additional requirements from new services. This growth rate exceeds the rate of increase in processing power and therefore results in an increase in the number of servers and the footprint of the datacenter. This rapid expansion of computing and data exchange capacity comes with an increase in power consumption, which is becoming a very important issue for present and future system deployment. It also results in increasing interconnect distances within datacenters. It is thus of paramount importance to develop more power-efficient communication solutions for datacenters for which transmission distance of interest are ranging from several meters up to 2 km. Supercomputers continue to grow at around 80% per year [31] and pose similar challenges to datacenters though they typically require lower latency and hence shorter distances but with higher interconnect bandwidth density.

Today multimode parallel interconnects represent the most cost-effective solution, and dominate this market with the bit-rates of 1–10 Gb/s. However the scalability of existing solutions is limited for several reasons. First, they are making use of vertical-cavity surface-emitting lasers (VCSELs), which are subject to the limitations imposed to direct modulation bandwidth in lasers. Currently available VCSEL commercial products are limited to 10 Gb/s and some research demonstrations have been made at 17 Gb/s-50 Gb/s. However, the available link span with optimized multimode fiber, such as OM3, is limited to about 300 m at 10 Gb/s and 70 m at 25 Gb/s. Secondly, it is very challenging to introduce WDM functionality in optical links using VCSEL sources, as this would impose a high price premium to VCSEL wavelength selection and complicated fiber coupling schemes for multimode fiber. While VCSEL devices can be used with single mode fiber, this removes many of advantages that packaging for multimode alignment tolerances bring. Hence, present VCSEL based solutions can only be scaled by increasing the number of fibers, which is problematic in datacenters where running multi fiber ribbons over long distances has significant cost and for density of interconnect in supercomputers, as with routers and switches.

For all these reasons, disruptive solutions taking advantage of WDM in SMFs are being actively looked at, with the goal of at higher transmission bit rates and extended reaches. Photonic integration on silicon combining active devices such as lasers and modulators, and passive building blocks, such as wavelength multiplexers, grating couplers, is widely perceived as the emerging solution for a cost-effective and scalable communication technology for datacenters/supercomputers.

We expect the bit rate per channel and the number of WDM channels will continue to grow in coming years, with the total capacity per link potentially reaching 1 Tb/s using a 40×25 Gb/s system. At the same time parallel SMFs or even fibers with multi single-mode cores can be used to increase further the total link capacity. However there may
exist several challenges to be overcome by silicon photonics before mass deployment:

1. Decrease of power consumption: this means that in particular silicon modulators with low drive voltage and power-efficient lasers without thermal coolers should be developed.

2. Co-integration of electronics and photonics: high capacity silicon PICs need to be connected with modulator drivers, transimpedance amplifiers (TIAs), control electronic circuits, etc. Cost-effective co-integration scheme should be developed to allow the exploitation of the potentials of silicon PICs.

3 Silicon photonic devices

In this section, we review a few silicon photonic devices developed at Bell Labs. These devices include modulators, hybrid lasers and polarization elements, which are building blocks for photonic integrated circuits.

3.1 Single-drive push-pull silicon MZMs

Electro-optic modulators are one of the most crucial devices in optical communication. The performance of a Mach-Zehnder modulator (MZM) can be determined by three most important parameters, the bandwidth (or speed), the voltage swing $V_\pi$ for a phase change of $\pi$ between the two arms of MZMs, and the insertion loss. Among the three parameters, reducing $V_\pi$ usually results in reduced bandwidth and increased insertion loss. However, for many current and future applications, it is highly desirable to have both higher bandwidth and lower $V_\pi$, driven by increasing data rates, lower power consumption, as well as difficulties to develop high-voltage amplifiers with broad bandwidths. This poses challenges for electro-optic modulators, especially for silicon modulators, which further suffer from the weak electro-optic effect in silicon.

High-bandwidth modulation in silicon can be realized by free-carrier induced index change [32]. The carrier-density modulation in a silicon waveguide can be obtained with carrier injection in a forward-biased $pin$ diode structure [33], carrier accumulation in a MOS capacitor structure [34], or carrier depletion in a reverse-biased $pn$ diode structure [35–40]. Carrier depletion has the weakest modulation efficiency, yet comes with the best high data rate performance, as doping profiles can be used to optimize junction capacitance. Recently, high data rates of 30–50 Gb/s have been demonstrated using carrier depletion [35–40]. However, most of the reported high-bandwidth silicon carrier-depletion MZMs were demonstrated by using devices with rather short phase shifters with an extremely high or impractical $V_\pi$. A typical $V_\pi$ for $>25$ Gb/s operation is larger than 7 V [35–40]. Compared with LiNbO$_3$ or InP modulators where a $V_\pi$ of 2–3 V can be achieved, the $V_\pi$ of silicon MZMs is much higher.

In [24, 38, 41], novel single-drive push-pull MZMs with low $V_\pi$ and high bandwidth were demonstrated by Bell Labs. The modulation of these MZMs is based on the carrier depletion of silicon $pn$ junctions embedded in the middle of silicon waveguides. A transmission-line electrode is loaded with the junction capacitor. Larger load capacitances make it more challenging to design the travelling-wave electrodes. A single-drive push-pull scheme can be employed to effectively reduce the capacitance in half, where both modulator arms are symmetrically doped and share a highly n-doped region in the center (see Figure 3A). Symmetric coplanar strips are connected with outside highly p-doped regions of two MZM arms. The central highly n-doped region is connected separately for $dc$ bias. Since the two junction capacitors in two MZM arms are connected in serial, the loaded capacitance on the transmission line is half of that for one arm (assume the capacitance are the same for both arms). This design

![Figure 3](image-url)

**Figure 3** Single-drive push-pull silicon MZM [38]. (A) Waveguide cross-section for high speed modulation. (B) Optical picture of a fabricated MZM. (C) Optical eye diagram at 30 Gb/s for a MZM with a $V_\pi$ of 3.1 V.
allows both arms to be driven in a push-pull fashion with a single input drive signal. Furthermore, the push-pull scheme reduces the modulation-induced frequency chirp. In [38], the $V_\pi$ was demonstrated to be as low as 3.1 V at a high data rate up to 30 Gb/s and 40–50 Gb/s modulations for shorter devices with higher $V_\pi$ were also demonstrated. The achieved $V_\pi$ is close to that demonstrated for LiNbO$_3$ and InP modulators, however, the insertion loss is relatively high due to free carrier induced loss from $pn$ junctions. In [41], the modulation chirp and dispersion tolerance of this type of modulators were presented.

3.2 Hybrid silicon/III-V lasers

The laser source is an important building block for PICs on silicon. Today, practical Si-based light sources are still missing, despite the recent demonstration of a germanium laser [42]. This situation has driven research to the heterogeneous integration of III-V semiconductors on silicon [2]. In order to densely integrate the III-V semiconductors with the silicon waveguide circuits, mainly adhesive and molecular wafer bonding techniques are used. In these approaches, unstructured InP dies or wafers are bonded, epilayer layers down, on a SOI waveguide circuit wafer, after which the InP growth substrate is removed and the III-V epilayer film is processed. Figure 4A shows a $2''$ InP wafer bonded to an 8” SOI wafer with patterned silicon waveguide structure. Figure 4B shows a scanning electron microscope (SEM) image of a hybrid silicon/III-V 1.9-µm laser after the III-V waveguides were fabricated on top of silicon waveguide, reported by Dong et al. from Bell Labs [43].

Duan et al. have developed hybrid silicon/III-V lasers exhibiting new features [44–48]. For instance, III-V waveguides have a narrow width of <3 µm, reducing the power consumption of the devices. In order to make the mode coupling efficient, both the III-V waveguide and silicon waveguide are tapered, with a tip width for the III-V waveguide down to 300 nm for some devices. Moreover, a widely wavelength tunable laser was demonstrated [44], as schematically shown on Figure 5A. This laser consists of an InP based amplification section, tapers for the modal transfer between III and V and Si waveguides, two ring resonators (RRs) for single mode selection, metal heaters on top of the rings for the thermal wavelength tuning and Bragg gratings providing reflection and output fiber coupling. In the silicon sections, ring resonators 1 (R1) and 2 (R2) have free spectral ranges (FSR) of 650 and 590 GHz, respectively. Figure 5B shows the superimposed laser emission spectra by changing heating power.
levels to the two RRs. On the backgrounds of those spectra curves, one can observe transmission peaks created by R2 and the transmission dips created by R1. With <400 mW of combined power in both heaters, a high wavelength range over 45 nm is achieved with side mode suppression ratio higher than 40 dB [44]. It was also demonstrated that those lasers exhibit excellent performance as local oscillator in a coherent receiver [47]. A tunable transmitter, integrating a hybrid silicon/III-V laser and silicon MZM was also reported [46]. The integrated transmitter exhibits 9-nm wavelength tunability by heating an intra-cavity ring resonator, high extinction ratio from 6 to 10 dB, and excellent bit-error ratio (BER) performance at 10 Gb/s [46].

3.3 On-chip polarization elements

The aforementioned submicron silicon waveguides have very different mode fields and effective indexes for TE and TM modes. This introduces significant challenges for polarization-insensitive applications such as WDM receivers. Polarization-diversified circuits can solve this challenge, however, on-chip polarization elements such as polarization rotators and polarization beam combiners/splitters (PBC/S) are demanded. In coherent optical transmission, the generation and detection of dual-polarization optical signals, which doubles the data capacities of fiber transmission, also requires these polarization elements. As discussed in Section 1, high-index-contrast silicon waveguides allow relatively easier design of polarization rotators and PBCs compared with other photonic technologies, since the waveguide modes are inherently hybrid modes and also the modal index/field can be controlled by the core size. Various silicon polarization rotators have been reported with high performance [10–14]. Both dual-layer and single-layer waveguide structures can be employed.

In realizing these importance, high-performance polarization rotators and PBCs were developed by Chen et al. from Bell Labs [12]. The polarization rotator is based on the adiabatic mode evolution as shown in Figure 6. The structure consists of a regular silicon waveguide with an additional silicon nitride (SiN) structure located on top of the silicon waveguide. The device rotates the TM polarization of a silicon waveguide to its TE polarization (or vice versa), allowing seamless integration with other silicon-based components. Shown in Figure 6A, with the first mode adapter, the TM mode of a regular silicon waveguide is transitioned to the TM mode of the combined structure with both Si and SiN having the same width. The width of the combined structure is chosen so that its TM fundamental mode has a higher index than its TE fundamental mode. In the rotator section, the silicon waveguide gradually increases its width, and at the same time the SiN waveguide gradually reduces its width and moves away from the silicon waveguide. At the end of the rotator, the TE fundamental mode now has a higher index than the TM fundamental mode. If the transition is slow enough to be adiabatic, each optical mode should maintain its mode order during the evolution. Another mode adapter is used here to connect the output of the polarization rotator to a regular silicon waveguide. To achieve a PBC/S, a silicon waveguide directional coupler can be employed. With same gaps, the TM-mode coupling between two adjacent waveguides can be significantly larger than that for TE. Using this property, it is feasible to design directional couplers which have >95% coupling efficiency for TM mode but <5% for TE mode. By combining PBSs with polarization rotators, Ref. [12] reported a polarization-diversified circuit with a 1.5 dB insertion loss and >30 dB polarization extinction ratios over a 60-nm spectral range.

4 Silicon photonic integrated circuits

Although many silicon photonic components have been demonstrated, the performance of most individual
devices is still worse than those from individually optimized devices in LiNbO$_3$, III-V semiconductors and silica. Nevertheless, as more optical functionality needs to be integrated in many applications, silicon photonics could offer a practical and flexible platform for PICs. Bell Labs has reported various PICs, indicating that silicon photonics could find more utility in photonic integration than in discrete devices. At receiver side, the demonstrated PICs include various WDM receivers [23, 49–51], dual-polarization coherent receivers based on novel gratings [21, 52] and on-chip polarization rotators [22], dual-polarization differential-QPSK (DQPSK) receivers [53], and space-division multiplexing (SDM) receivers [54]. At transmitter side, the demonstrated PICs include 10×25 Gb/s dense WDM (DWDM) modulators [24], dual-polarization coherent modulators based on silicon MZMs [20], QPSK modulators based on microring modulators [55, 56], and DWDM 10-channel variable optical attenuators with multiplexers (VOA-MUX) [57]. In this section, we review some of them.

It is to be noted that both InP and silicon PICs are very promising in various applications, each with their own merits and limitations. InP PICs can provide integrated lasers, but it is challenging to integrate lasers, modulators, photo detectors and polarization elements all on a single chip. Moreover, its yield and cost could be concerns. Silicon PICs take the advantage of CMOS foundries with large wafers, high yield and low cost. As mentioned earlier, silicon waveguides also have the flexibility to implement polarization combiners and rotators, which offers advantages on polarization diversity circuits. With the emerging hybrid wafer-scale integration technology to bond InP on silicon [2], it is also feasible to support integrated amplifiers and lasers.

### 4.1 WDM receivers

High-index-contrast silicon waveguides have many advantages, but with a severe drawback: the effective index is very sensitive to fabrication variations. This translates to the phase uncertainty of an optical signal propagating through the waveguide and induces significant challenges to achieve accurate wavelength controls for narrow-bandwidth devices such as microrings and WDM filters. Our approach is to use SiN waveguides to reduce the index contrast with oxide cladding. For this purpose, a silicon/SiN integration platform has been developed to implement various WDM PICs. The SiN is deposited on top of silicon waveguides by low-pressure chemical vapor deposition. By properly designing the transition tapers between silicon and SiN waveguides, coupling loss can be on the order of 0.1 dB. Using the same platform, polarization rotators can be realized, as explained in the previous section.

The demonstrated WDM receivers include a polarization-insensitive two-wavelength receiver for access applications [51], a 40-channel 40 Gb/s WDM receiver [23], a polarization-diversified DWDM receiver [49], and a monolithic diplexer [50]. For these receivers, germanium photo detectors by epitaxial growth on silicon waveguides were employed [58]. In Ref. [51], Chen et al. reported a polarization-insensitive two-channel receiver which utilizes a novel polarization-insensitive SiN Mach-Zehnder interferometer (MZI) and integrated germanium photo detectors. A fiber-to-detector polarization-dependent loss of <0.8 dB was demonstrated over a wide wavelength range. By packaging the receiver chip with TIAs, sensitivities of 23.3 and 22.6 dBm for the two channels at 2.5 Gb/s were demonstrated. In Ref. [23], Chen et al. reported a 40-channel monolithically integrated receiver PIC on silicon, which consists of a SiN arrayed waveguide grating (AWG) with integrated germanium photo detectors. Net responsivities from a cleaved standard single-mode fiber to detectors of 0.15–0.22 A/W were measured, with flattened passbands with 1-dB bandwidth over 60% of the 200-GHz channel spacing. Single-channel operation up to 40 Gb/s was demonstrated with a wire-bonded TIA (see Figure 7A). This receiver, however, only works for TE mode. In Ref. [49], Chen et al. further demonstrated a monolithically integrated, polarization-diversified silicon receiver chip with 10 wavelength channels at 100-GHz spacing. It has <1.8 dB polarization-dependent loss and zero polarization-dependent wavelength shift. On-chip polarization rotators have been used to convert the TM component in an optical signal to TE mode, which is demultiplexed by the same AWG as for the TE component.

### 4.2 WDM transmitters

Integrating the single-drive push-pull MZMs and a SiN AWG, Chen et al. further demonstrated a DWDM 10×25 Gb/s modulator chip with a footprint of only 5×8 mm$^2$ [24]. The SiN AWG has 100-GHz channel spacing. The MZMs have a $V_r$ of ~10 V. With a drive voltage of 6 V and a 3 V reverse bias, the achieved dynamic extinction ratios are 5.6–7.2 dB for the modulators with a total on-chip insertion loss of about 5 dB for all ten channels. Including the coupling loss to fibers and the AWG loss, the total insertion loss is ~18.5 dB. Figure 7B shows the chip layout and the optical eye diagrams of all ten channels at a data rate of 25 Gb/s after the AWG multiplexer.
4.3 Coherent receivers

Optical coherent receivers, which convert the amplitude, phase, and polarization of an optical field signal into the electrical domain, include a number of optical components, such as polarization splitters, 90° optical hybrids and photo detectors. These components are ideally implemented on PICs with the advantages of accurate optical path control, compact size, and low packaging cost. The fundamental concept for coherent detection is to measure the product of electrical fields from a modulated signal and a continuous-wave (CW) local oscillator (LO). Mixing the signal and LO using a 2×2 coupler can do this, for example. To suppress dc components, balanced detection is usually employed at the two outputs. With such 2×2 coupler, however, only one quadrature information of the signal can be measured. Equivalently, the complex amplitude, which consists of both magnitude and phase, of an electrical filed cannot be extracted by a single photo-current measurement. In order to achieve complex amplitude, one can use optical 90° hybrids, which mix the signal and LO with four outputs, for which 0°, 90°, 180°, and 270° phase shifts between the signal and LO are introduced. For a dual-polarization signal, a polarization-diversified scheme is required. A generic circuit diagram of such coherent receiver is shown in Figure 8A. Two PBSs are used to split the signal and LO into TE and TM components. The TE (or TM) components of signal and LO are mixed with a 90° optical hybrid, balance-detected by four photo detectors and amplified by two TIAs, which produce both in-phase and quadrature information of the signal. Such coherent receivers have been realized in discrete component formats, hybrid planar lightwave circuits with photo detectors [59–61], InP PICs [62–64], and silicon PICs [21, 22]. Except silicon PICs, polarization diversity or dual-polarization coherent receivers are realized by the use of micro-optical free-space polarization rotators and beam splitters.

In Ref. [21, 22], two types of dual-polarization coherent receivers were demonstrated based on silicon PICs from Bell Labs. Doerr et al. demonstrated a grating-assisted
coherent receiver PIC [21, 52], where a 2-dimensional (2-D) grating is used for fiber coupling, polarization splitting and 50/50 power splitting. A 2-D grating coupler is a photonic crystal that couples a wave traveling normal to a substrate to a wave guided parallel to the substrate (see the inset of Figure 8B). Light incident on the grating from the vertical direction is phase-matched to waveguide guiding modes in a certain direction at the designed wavelength and polarization. With these gratings, the TE and TM components of signal (and LO) can be coupled and separated into different silicon waveguides. Once coupled in, all of the light on the chip is TE polarized. The coupled signal and LO pass through two 90° hybrids based on 2×2 multi-mode interferometers (MMI) and eight photo detectors. The principle of coherent detection is the same as explained for Figure 8A. Using this PIC, Doerr et al. successfully detected a 112-Gb/s PDM-QPSK signal, with BER performance comparable to a commercial coherent receiver [52].

In Ref. [22], Dong et al. implemented a silicon coherent receiver by integrating on-chip polarization rotators and splitters. Shown in Figure 8C, the optical signal enters the PIC from one facet with two polarizations. The optical LO is coupled into the Si PIC from the other facet. Once coupled in, the signal and LO are divided into TE and TM polarizations by two PBSs. The TE polarized lights proceed to the 4×4 MMI-based 90° hybrids, whose four outputs are detected by four germanium photo detectors on the left side of the PIC (see Figure 8C). The balance detection between the first and fourth photo detectors produces the in-phase TE-polarization components, and the second and third photo detectors produces the quadrature TE-polarization components. The TM components from the output of PBSs are converted to TE polarization by two polarization rotators. The converted TE lights enter the right-side 4×4 MMI-based 90° hybrid, which is identical to that for the TE mode. The in-phase and quadrature in the TM-polarization components are produced with the same balance detection scheme as those for the TE mode. Using this PIC co-packaged with TIAs, Dong et al. successfully detected a 112-Gb/s PDM-QPSK signal and a 224-Gb/s PDM-16-QAM signal [22].

4.4 Coherent transmitters

A coherent modulator encodes electrical signals on both the amplitude and phase of a light wave. Such modulator is called in-phase/quadrature (I/Q) modulator or a vector modulator. A basic I/Q modulator consists of a pair of MZMs and a power combiner which combines the two MZMs outputs with a π/2 phase difference, from which the real and imaginary components of an optical wave can be manipulated independently. Multi-level QAM signal can be synthesized by using parallel I/Q modulators, or by a single I/Q modulator with multi-level electrical driving signals. Figure 9A shows a circuit diagram for a dual-polarization I/Q modulator. In order to achieve dual polarizations, two I/Q modulators or four MZMs are integrated together with a polarization rotator and a PBC. Current dual-polarization I/Q modulators in long-haul optical systems use discrete optical components such as LiNbO₃ modulators with free-space or fiber polarization multiplexers. Integrated approaches have been demonstrated where silica or polymer PLCs are assembled with LiNbO₃ or InP modulators [65–67]. Single-polarization I/Q modulators have been also demonstrated by monolithic InP or GaAs PICs [68–70]. However, monolithic PICs for dual-polarization I/Q modulators have not been achieved in InP PICs, to the best of our knowledge.

Recently, Dong et al. presented QPSK modulation based on nested signal-drive push-pull silicon MZMs [71]. A 50-Gb/s QPSK signal was generated with only 2.7-dB optical signal-to-noise ratio (OSNR) penalties from the theoretical limit at a BER of 10⁻³. Compared with commercial LiNbO₃ I/Q modulators, there is only ~1 dB OSNR penalty.
penalty. This is the first successful demonstration of advanced modulation formats using silicon MZMs. By further integrating two I/Q modulators and an on-chip polarization rotator and PBC, Dong et al. further implemented a monolithic single-chip dual-polarization coherent modulator to generate a 112-Gb/s PDM-QPSK\[20\] and a 224-Gb/s PDM-16-QAM signal [22]. In [20], Dong et al. showed that the integration of on-chip polarization elements introduces an additional 0.9-dB penalty due to polarization dependent loss. To the best of our knowledge, this PIC is the first monolithic single-chip dual-polarization I/Q modulator, with highest photonic integration in this particular application. Single-polarization silicon I/Q modulators were also reported from other groups/companies with comparable performance to those LiNbO$_3$-based coherent modulators [72–74]. Combining the dual-polarization silicon I/Q modulators and the silicon receiver based on on-chip polarization elements, Dong et al. reported a 2560-km SFM transmission of a 112 Gb/s PDM-QPSK signal [75], validating the readiness of silicon PICs in optical coherent links.

High-bandwidth advanced modulation signals can be also realized in silicon microring modulators, which hold the promise to achieve extremely low power consumption due to their micron-meter sizes [33, 76–79]. The resonant transmission of a microring comes with a dramatic phase change around the resonant wavelength. For single-waveguide-coupled rings, the over-coupling condition (i.e., power couplings between bus waveguides and rings are larger than the round-trip loss of the rings) results in a monotonic phase change from 0 to $2\pi$ across the rings’ resonant wavelengths. A proper resonance shift can generate a $\pi$-phase change while maintaining the same transmitted power at a prescribed wavelength, to produce a binary phase-shift-keying (BPSK) signal. If two BPSK ring modulators are nested in an MZI configuration, the QPSK modulation can be realized when there is a $\pi/2$ phase difference between two arms. In Ref. [55, 56], Dong et al. demonstrated a 56-Gb/s QPSK modulation using nested depletion-mode microring modulators with a ring radius of 30 μm and a PIC size of 0.25 mm × 2.5 mm. If two polarizations are used, 112 Gb/s can be achieved, which are suitable for 100-Gb/s channel rates.

5 Conclusions

In this paper we have reviewed recent achievements in silicon photonic devices and integrated circuits from Bell Labs. From its technical advantages, we believe that silicon photonics is well suited for various applications, which require disruptive optical technologies for high bandwidth, high bandwidth density, energy efficient and low cost information transmission. The discussed applications include long-haul/metro optical coherent networks, optical interconnects for routers and switches and short-reach communications in datacenters and supercomputers. Driven by these applications, many high-performance silicon devices and PICs have been reported from Bell Labs. Here, we have particularly discussed single-drive push-pull silicon MZMs, SiN-assisted polarization rotators, hybrid silicon/III-V lasers, silicon/SiN integrated AWGs, WDM transmitters/receivers, and dual-polarization coherent transmitters/receivers, which are unique and important contributions to this field from Bell Labs. While individual device fabricated in silicon photonic rarely exceed the performance of discrete optimized components, this should not discourage the effort to integrate them as this was also the case with early electronic integrated circuits, and the ability to provide large-scale integration can be used to mitigate or compensate these limitations. The demonstrated optical functions, high data capacities and dense integration verify silicon photonics could be a viable and powerful platform for numerous communication applications.

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